An integrated controller for an active magnetic bearing system

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by

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DECLARATION

I hereby declare that all the material incorporated in this thesis is my own original unaided work except where specific reference is made by name or in the form of a numbered reference. The word herein has not been submitted for a degree at another university.

Signed: _____

Jacques Jansen van Rensburg

SUMMARY

An active magnetic bearing (AMB) involves the suspension of a rotor by means of electromagnetic actuators. An AMB system comprises actuators, position sensors, a controller and power amplifiers. Conventional position sensors for rotor position sensing are expensive. The McTronX Research Group at the North-West University is currently conducting research on self-sensing, a method of extracting rotor position from the current and voltage actuation signals of the AMB.

It was deemed necessary to develop a complete platform that will enable the implementation of self-sensing algorithms. The platform incorporates analogue circuitry, embedded devices and switching power amplifiers. The system will thus integrate all the electronics required for AMB suspension, and is thus dubbed: an Integrated Controller.

The development of the integrated controller presented unique design challenges not yet faced by the McTronX group. To increase the chances of success and minimize some of the risks, the integrated controller was developed in collaboration with an industry partner.

The collaboration required a systems engineering approach to the project. A detail type B specification was drawn up to aid in the project management process. The specification includes important detail such as the functional architectures, functional capabilities, performance specifications and physical constraints of the integrated controller.

Some self-sensing algorithms can be implemented by means of analogue circuitry, and some can only be implemented in the digital domain. These digital algorithms are computationally intensive and require powerful processors. Digital signal processors (DSPs) and field programmable gate arrays (FPGAs) both exhibit unique architectures ideal for digital signal processing. Both these devices were implemented in the integrated controller, with the DSP as the main processor and the FPGA the co-processor.

Although the integrated controller can operate as a stand-alone system, it has several communication interfaces (RS485, USB and RS232). This allows the system to work in conjunction with other integrated controllers, to be controlled by a master controller or to communicate to a personal computer (PC).

Testing the integrated controller involved the closed loop current control of an AMB power amplifier, facilitating all critical functional aspects. The integrated controller's performance meets the required specifications and is expected to successfully facilitate future self-sensing investigations.

OPSOMMING

'n Aktiewe magnetiese laer (AML) behels die suspendering van 'n rotor deur middel van elektromagnetiese aktueerders. 'n AML stelsel bestaan tipies uit aktueerders, posisiesensors, 'n beheerder en kragversterkers. Die konvensionele sensors wat gebruik word om rotorposisie te bepaal is baie duur. Die McTronX navorsingsgroep by die Noordwes Universiteit is tans besig om self-waarneming na te vors, 'n metode om die rotorposisie af te lei vanaf die spanning en stroom aktueerseine van die AML.

'n Behoefte vir 'n platform waarop self-waarneming algoritmes geïmplementeer kan word, het ontstaan. Die platform integreer analoogelektronika, ingebedde beheerders en skakelmodus kragversterkers wat al die benodige komponente uitmaak van 'n AML beheerstelsel. Die platform is dan sodanig 'n geïntegreerde beheerder gedoop.

Die ontwikkeling van die geïntegreerde beheerder het 'n paar unieke uitdagings aan die McTronX groep gestel, sommige waarmee die groep nog nie te doen gehad het nie. Om die suksesvolle afhandeling van die projek te verseker, is 'n paar van die risiko's verminder deur die geïntegreerde beheer te ontwikkel in samewerking met 'n industriële vennoot.

Die projek is benader uit 'n stelsel ingenieurs oogpunt wat onder andere die opstelling van 'n tipe B spesifikasie behels het. Die spesifikasie sluit onder andere detail in soos funksionele argitekture, operasionele funksies, werkverrigting spesifikasies en fisiese beperkinge van die geïntegreerde beheerder.

Sommige self-waarnemings algoritmes kan met behulp van analoogelektronika uitgevoer word en ander slegs met die hulp van digitale beheerders. Die digitale algoritmes benodig kragtige prosesserings vermoë wat deur 'n digitale seinverwerker (DSP) en/of 'n *field programmable gate array* (FPGA) bevredig kan word. Altwee die toestelle is op die geïntegreerde beheerder geïmplementeer; die DSP as die hoofverwerker en FPGA as die hulpverwerker.

Alhoewel die geïntegreerde beheerder kan funksioneer as 'n alleenstaande stelsel, beskik dit oor verskeie kommunikasie-intervlakke (RS485, RS232, USB). Dit stel die stelsel in staat om te kommunikeer met ander geïntegreerde beheerders, om beheer te word deur 'n meesterbeheerder of om te kommunikeer met 'n persoonlike rekenaar (PC).

Die evaluering van die geïntegreerde beheerder het behels die sluiting van 'n AML kragversterker stroom lus. Al die kritiese aspekte van die geïntegreerde beheerder is deur hierdie metode geëvalueer. Daar word verwag dat die geïntegreerde beheerder voldoende sal wees vir self-waarneming ondersoeke aangesien dit aan die basiese spesifikaies voldoen.

ACKNOWLEDGEMENTS

A special thanks to M-Tech Industrial and THRIP for funding this research and granting me the opportunity to further my studies.

I would also like thank the following people who's contributions were invaluable during the course of this project.

- Professor George van Schoor, my supervisor, for his guidance, advice and for laying the foundations for the success of this project.
- André Niemann, my assistant supervisor, for his dedication, guidance and advice.
- Rob Hudson, who provided technical expertise, support and hours spent on design central to the success of this project.
- My family, for their unwavering love and support.

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"I can do everything through Him who gives me strength." Philippians 4:13

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LIST OF ABBREVIATIONS

ABS	Absolute value
ADC	Analogue to digital converter
AMB	Active magnetic bearing
ASIC	Application specific integrated circuit
BPF	Band pass filter
CAN	Controller area network
CCS	Code composer studio™
CLB	Configurable logic block
CMOS	Complementary metal-oxide semiconductor
CPLD	Configurable logic devices
CPU	Central processing unit
DAC	Digital to analogue converter
DPR	Dual port RAM
DSP	Digital signal processor/processing
EMIF	External memory interface
F x.x	Function number x.x
FFT	Fast fourier transform
FIR	Finite impulse response
FPGA	Field programmable gate array
FU x.x	Functional unit number x.x
GPP	General purpose processor
HSTL	High speed transistor logic
I/O	Input/Output
IDE	Integrated development environment
IGBT	Insulated gate bipolar transistor
ISE	Integrated software environment
JTAG	Joint test action group
kbps	Kilo bits per second
LPF	Low pass filter
LVDS	Low voltage differential signalling
LVPECL	Low-voltage positive emitter-coupled logic
LVTTL	Low-voltage transistor-transistor logic
MAC	Multiply and accumulate
Mbps	Mega bits per second
McBSP	Multichannel buffered serial port
MIPS	Million instructions per second
Msps	Million samples per second
PA	Power amplifier

PCB	Printed circuit board
PCI	Peripheral component interconnect
PID control	Proportional plus integral plus derivative control
PWM	Pulse width modulation
RAM	Random access memory
ROM	read only memory
RSDS	Reduced swing differential signalling
RTL	Register transfer level
SBC	Single board computer
SCI	Serial communication interface
SPI	Serial peripheral interface
SSTL	Stub series terminated logic
TI	Texas instruments
UART	Universal asynchronous receiver-transmitter
USB	Universal serial bus
VHDL	VHSIC hardware descriptive language
VHSIC	Very high speed integrated circuits
VLIW	Very long instruction word

LIST OF SYMBOLS

A, A_g	Cross sectional area of stator and air gap respectively
C	Capacitance
g	Air gap length
i	Current through coil
$I(s)$	Load current
K_P, K_I, K_D	Proportional, Integral and Derivative gain of PID controller respectively
L	Coil inductance
l_c	Magnetic path length
N	Number of coil turns
R	Electrical resistance
$\Re$	Total reluctance of magnetic circuit
$\Re_c$, $\Re_g$	Reluctance of core material and air gap respectively
T	Sampling period
t_r	Rise time
t_{ui}	Unit interval
v	Voltage across coil
V_b	Rail supply
$V(s)$	Load supply

Z_0	Characteristic impedance
ω_s	Sampling frequency
ω_{wp}	Pole frequency for digital PID control
ϕ	Magnetic flux

Chapter 1

Introduction

Chapter 1 presents some background on active magnetic bearings (AMBs) and gives the problem statement for this thesis. An overview of the issues to be addressed and methodology is also presented, after which an overview of the document is given.

1.1 Background

Active magnetic bearings (AMBs) comprise mechanical, electrical and electronic components that classify them as mechatronic products. This type of bearing is unique in the sense that there is no contact between rotor and actuator since the rotor is suspended using electromagnets.

Bearing stiffness, damping, rotor position and many other features can be actively controlled hence the name active magnetic bearings. These characteristics and a range of other advantages make AMBs attractive for application in turbomachinery, vacuum techniques, vibration isolation and application in space physics to name just a few [1].

1.1.1 Basic active magnetic bearing operating principle

The active magnetic bearing constitutes three main parts: the actuators, position sensors and controller. The sensor measures deviation of the rotor from the reference position whilst the controller uses the sensor output to derive a control signal for the power amplifiers. The power amplifiers convert the control signal to a corresponding current. This current energises the electromagnets of the bearing to create an attractive force.

Figure 1.1 illustrates a simple representation of an AMB. In the figure an analogue to digital converter (ADC) and a digital to analogue converter are represented in the controller box. This

is consistent with the use of a digital controller. Digital controllers have a number of advantages over the use of an analogue controller.

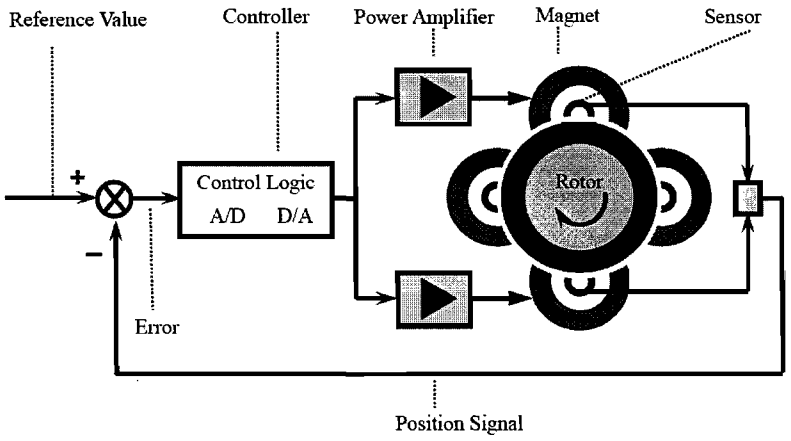


Figure 1.1: Representation of AMB system [2]

1.1.2 Digital Controller

Digital control is a preferred choice in today's digital society. Digital control presents advantages that renders it far more attractive than analogue control. Higher functionality can be achieved by using digital control rather than analogue control. The following are examples of functions that digital control can provide [1]:

- Procedures at start-up and shut down;
- Unbalanced treatment;
- Various filtering;
- Diagnosis;
- Monitoring.

Other advantages include [1]:

- More complex algorithms can be evaluated using digital control, which are impossible with analogue circuits;
- Digital control will reduce the susceptibility of noise on the system;
- Greater flexibility in the control algorithm implementation;
- Easier parameter adjustment;

- Real time monitoring and recording of operating conditions;
- Calibrating inputs are easier;
- Digital controllers reduce the amount of dedicated hardware, which make circuits more compact.

1.1.3 System architecture

The McTronX research group possesses an AMB model that is controlled by a rapid prototyping control system called dSpace®. The dSpace® hardware consists of a controller card that slots into a PCI slot of the PC. The card has several digital and analogue inputs/ouputs (I/O) and has a microcontroller on-board. It has certain shortcomings such as it requires a PC and cannot function as a stand-alone system.

Current system

The dSpace card and software are specifically designed to enable real time control and monitoring of a system. The dSpace software is integrated with the MATLAB® and Simulink® environment, as illustrated in Figure 1.2. ControlDesk® is part of dSpace software which provides the functionality to control, monitor and automate experiments.

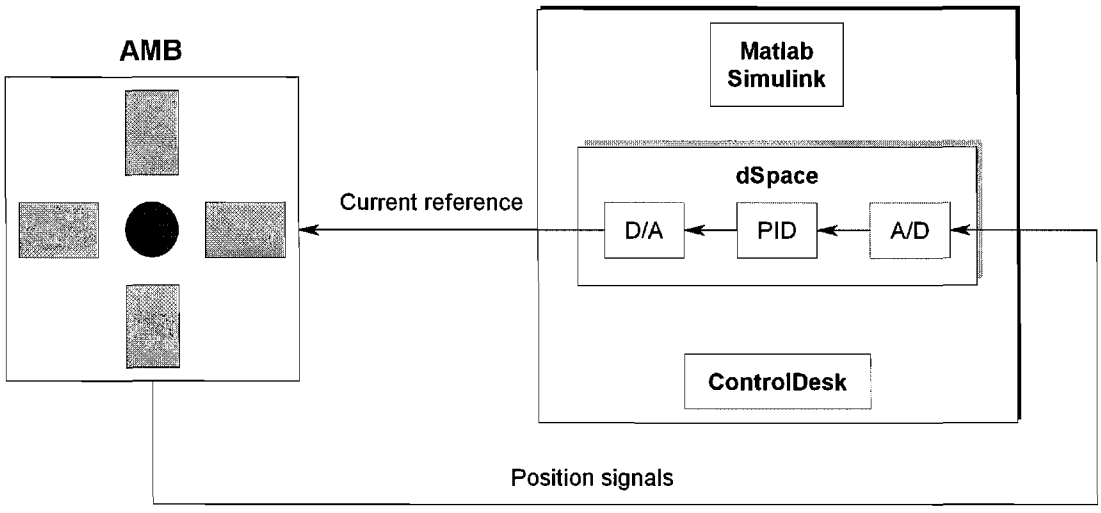


Figure 1.2: Current AMB control system configuration

Proposed system

Traditional AMB systems commonly use eddy current sensors for rotor position sensing. These sensors are expensive and contribute to a large portion of the total cost of an AMB system. Different techniques are being researched for determining the rotor position from the currents through the electromagnets of the AMB (see section 2.1). This is called self-sensing [3].

An integrated controller is to be developed that will be used to implement different self-sensing techniques, for differential drive mode. The model requires two power amplifiers for one degree of freedom. For example, vertical suspension requires a power amplifier for the top electromagnet and one power amplifier for the bottom electromagnet. Each integrated controller will have an embedded device for executing control algorithms and two power amplifiers.

Figure 1.3 illustrates a proposed configuration that utilizes integrated controllers. An integrated controller will be able to function as a stand-alone controller. By connecting multiple integrated controllers with each other, more complex control algorithms can be implemented and evaluated. This configuration will require a high speed communication bus between integrated controllers.

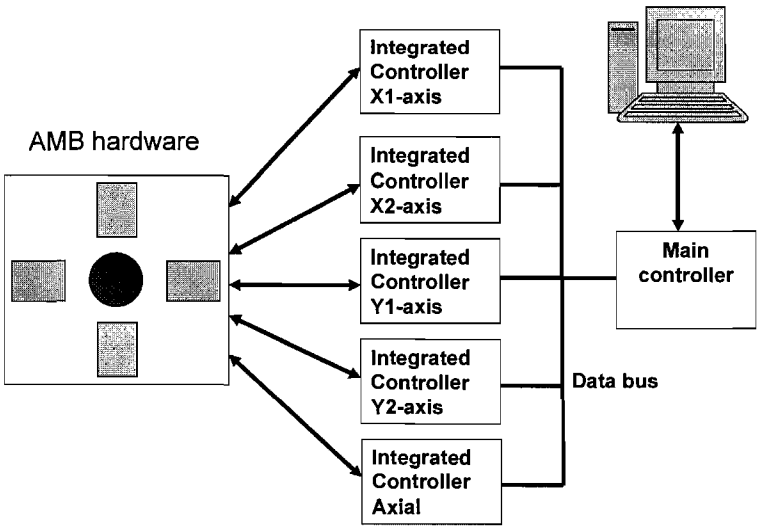


Figure 1.3: Proposed AMB control system configuration

1.2 Problem statement

The purpose of this project is to develop an integrated controller for the purpose of providing an optimal platform for implementing and evaluating self-sensing techniques.

Each integrated controller shall be able to suspend the AMB in one degree of freedom and can be duplicated for the suspension of an AMB in multiple degrees of freedom.

The integrated controller will consist of analogue, digital and power electronics. A circuit board layout that incorporates analogue, digital and power components poses some unique design issues.

The embedded devices located on the integrated controllers must be able to execute algorithms including DSP functions such as filters and FFTs within specified time constraints.

1.3 Issues to be addressed and methodology

The integrated controller is to be developed in collaboration with an industry partner. The decision to take this approach was based on the following:

- The McTronX group has a lack of experience in the development of digital hardware architectures. The industry partner on the other hand offers resources in terms of experienced designers as well as tested and verified functional designs.
- Detail design, and design verification were done by both the industry partner and McTronX. This ensured reliability and provided both the industry partner and MctronX insight into certain design issues.
- The MctronX group has the chance to gain valuable experience for future designs. Working with an external company requires detail project management for successful end-product development. McTronX research group will have knowledge on successful planning and management for collaborative projects.
- The collaboration between a well funded research group and a company adhering to very high development standards ensured a high quality end-product.

1.3.1 Conceptual analysis

Certain aspects had to be considered in the conceptual analysis before the specification could drawn up. The following aspects will be briefly discussed: communication architectures, embedded devices, circuit design and printed circuit board (PCB) layout, firmware development.

Communication architectures

High speed communication has to be established between integrated controllers to relay data such as rotor position, reference current, status information etc.

Protocols and interface schemes will be considered and weighed against each other for robustness, speed, bus architecture capabilities etc. Common interfacing schemes typically used to connect controllers are: RS485, RS422, RS232 and CAN [4],[5],[6].

Embedded devices

The control scheme for the AMB determines the type of embedded device. The digital signal processor (DSP) and Field Programmable Gate Array (FPGA) each has their advantages, disadvantages and unique features that have to be considered in the design process.

Research data will be collected and tests conducted on available devices in order to evaluate embedded devices. Some considerations for the choice of the embedded device include: learning curve for using device, algorithms to be implemented on the device, device processing speed, device architecture etc [7].

Circuit design and printed circuit board (PCB) layout

The integration of an embedded device with the power amplifiers will require careful circuit design. Circuit design will involve digital, analogue and power circuits. Analogue circuits will include analogue to digital converters (ADCs), filters and power supply circuits. The digital circuits will incorporate external RAM, the embedded device itself, communication line drivers and other peripheral circuits. The power circuit will incorporate switching devices in two- and three-phase bridge topologies.

Once a circuit layout has been designed, the circuit need to be etched on a PCB. A PCB layout design for such a complex system demands time and experience. Issues to be considered in PCB layout include, proper grounding, filtering, shielding and cabling to name just a few[8].

The circuit design and PCB layout in the development of the integrated controller has been identified as high risk factors. In order to reduce the risk the design of the digital circuitry, PCB layout and integration will be sub contracted to the industry partner.

Firmware development

In combination with the development of the hardware for the integrated controller, firmware has to be designed and implemented on the embedded devices.

The firmware for the embedded device will then be coded in an appropriate language and compiler. If a Texas Instruments (TI) DSP device is used, Code Composer Studio (CCS) will be utilized for firmware development. For Xilinx FPGAs, Xilinx's ISE will be used for firmware development in VHDL.

For development and testing purposes it is useful to know what is happening in the embedded code of the embedded device in real time. Emulation devices are available that enable the real time monitoring and controlling of firmware.

1.3.2 System specification

A system specification will be compiled. The specification will include technical guidelines for the development of the integrated controller. The compiled specification will be distributed to a sub-contractor to provide guidelines for the hardware development.

The project will thus be managed by performing system engineering functions which will constitute part of the study.

1.3.3 Sub-system procurement

Four sub systems have been identified: the power amplifiers, the digital electronics, analogue electronics and firmware. Each of these sub systems need to be developed and integrated.

1.3.4 System integration

Each sub-system, power amplifiers, digital electronics, analogue electronics and firmware has to be integrated to constitute the complete system of the integrated controller.

The system specification will ensure that all sub-components can be properly integrated by specifying the interfaces and their technical requirements. The integration of the sub-systems will also constitute part of this study.

1.3.5 System evaluation

The integrated control system for the AMB has to be evaluated and tested. Predicted results will be evaluated with the use of measurements and inspection. The system can then be characterized and verified using the tests results obtained. Recommendations and conclusions will be derived.

1.4 Document overview

A brief overview of this thesis will now be given:

1.4.1 Chapter 2: Literature study

Chapter 2 will present detail on literature knowledge obtained through the course of this thesis. Aspects such as self-sensing, embedded devices, communication interfaces and systems engineering will be addressed.

1.4.2 Chapter 3: System specification

A detail specification was drawn up for the development of the integrated controller. The specification is a combination of a type A and B specification. In Chapter 3 an adapted version of the specification is presented to help guide the reader's understanding of the integrated controller's structure and functions.

1.4.3 Chapter 4: Sub-system design and evaluation

In the specification certain choices were made regarding functional architecture units. Chapter 4 strives to motivate these choices, specifically the choice of embedded devices and the communication interface. An experimental laboratory configuration evaluates RS485 communication. Theoretical predictions are made in the amount of processing power that will be required for the implementation of certain algorithms that the integrated controller will be designed to execute.

1.4.4 Chapter 5: Integrated controller hardware and evaluation

Chapter 5 presents the integrated controller hardware. Key components of the hardware are marked and referenced back to the specification to show traceability from specification to actual product. The integrated controller is then evaluated. First the sub-components are evaluated and then the complete system is integrated and evaluated.

1.4.5 Chapter 6: Conclusions and recommendations

Chapter 6 concludes that the integrated controller's evaluation reveals compliance to the specification. Recommendations for future work is also discussed.

Chapter 2

Literature study

Chapter 2 provides details on aspects that played a key role in the development of an active magnetic bearing. Because self-sensing research is the main driving force behind the development of the integrated controller, some aspects of self-sensing will be discussed. Furthermore processors, communication interfaces and systems engineering will enjoy attention. Systems engineering will be applied since the integrated controller is developed in collaboration with an industry partner.

2.1 Self-sensing

In a traditional AMB system the rotor position is determined with the use conventional sensors. Expensive eddy current sensors are commonly used in AMB applications. Self-sensing strives to eliminate these sensors and extract the position information using alternative techniques. Self-sensing provides some advantages. To name a few [3]:

- Fewer components in the system implies fewer components that can malfunction.
- In smaller systems the cost is reduced significantly by eliminating dedicated position sensors
- Self-sensing could be used as a backup measure when sensor failure occurs (redundancy).

There are basically two main types of self-sensing techniques as illustrated in Figure 2.1, state estimation and modulation. This thesis concentrates on developing hardware suitable for implementing modulation based self-sensing.

The modulation based self-sensing technique is based on extracting the position information from the currents and voltages in the electromagnetic coils. Figure 2.2 shows a block diagram representation of a modulation self-sensing setup for one degree of freedom on the AMB.

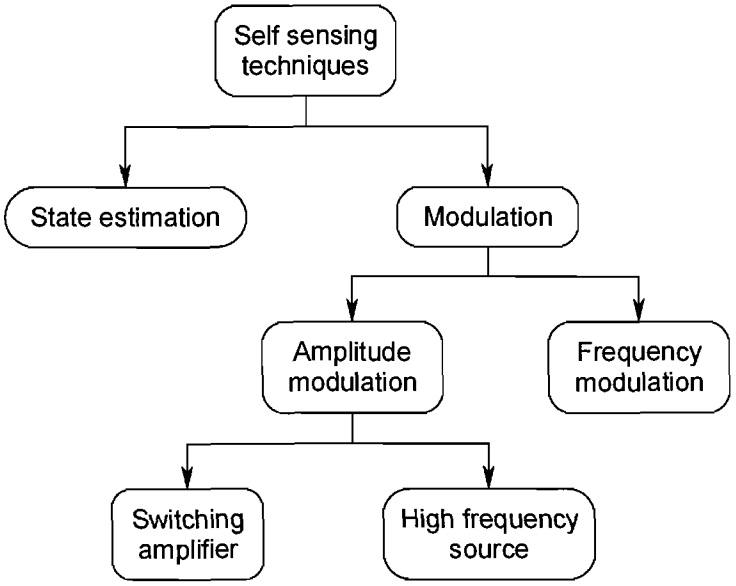


Figure 2.1: Types of self sensing [3]

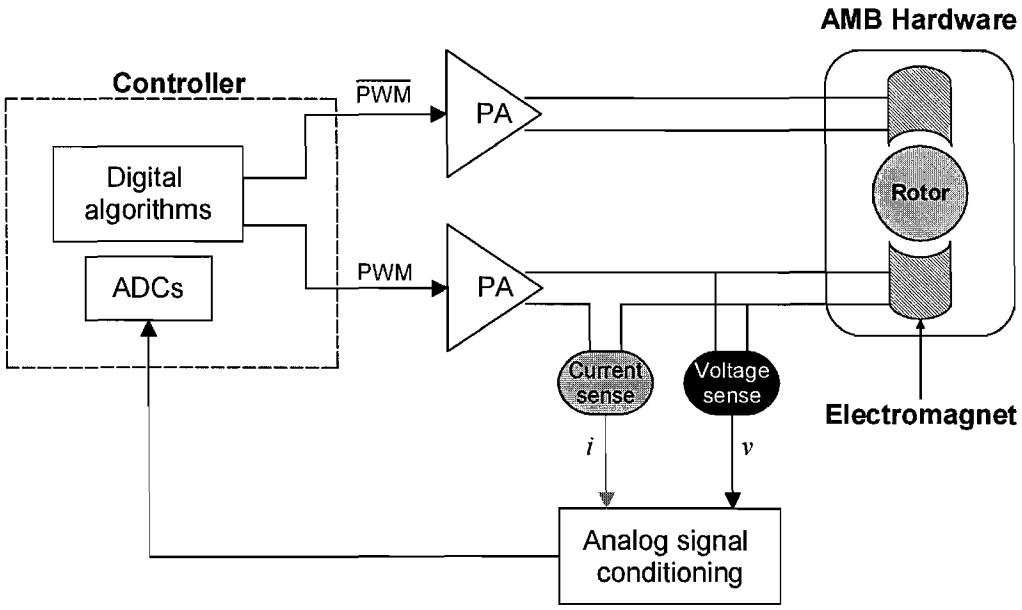


Figure 2.2: AMB self-sensing setup

2.1.1 Basic magnetic bearing model

To motivate the study into the self-sensing technique further, a simple model for a magnetic bearing will now be derived. The model is adapted from the work of Schammass [3]. This will illustrate the relationship between the changing current in the electromagnetic coil and the position of the rotor. The magnetic circuit in Figure 2.3 is considered.

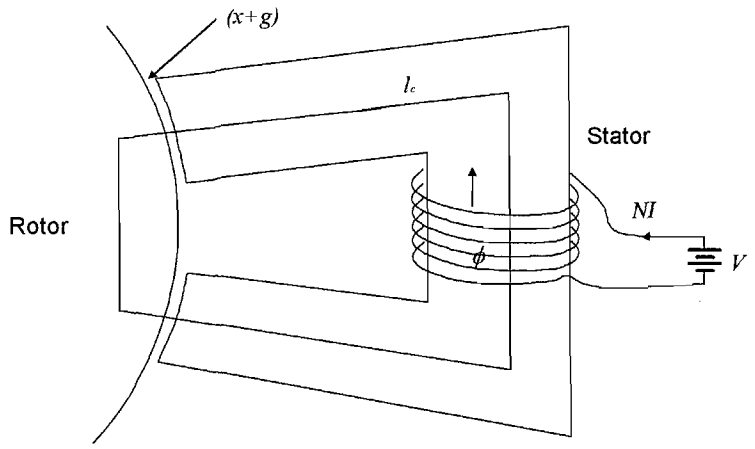


Figure 2.3: Magnetic circuit

Applying Faraday's law of inductance to the circuit, (2.1) can be formulated

$$v = N\frac{d\phi}{dt} + iR \tag{2.1}$$

with:
v : voltage across the coil;
N: number of turns;
R : coil resistance;
ϕ : flux;
i : current in coil.

The equation for flux is given as

$$\phi = \frac{Ni}{\Re} \tag{2.2}$$

where $\Re$ is the reluctance of the magnetic circuit.

For this circuit the reluctance is divided into two parts; the reluctance of the air gap and the reluctance of the magnetic material. By summing the two reluctances (2.3) is obtained.

$$\Re = \frac{2(g \pm x) + {}^{l_c}/_{\mu_r}}{\mu_0} \tag{2.3}$$

With:
g : nominal air gap;
x : change in the air gap;
A : cross sectional area of stator;

l_c : magnetic path length;
μ_r: relative permeability of material.

The inductance of the coil is calculated as follows:

$$L = N\frac{\partial\phi}{\partial i} = \frac{\mu_0 N^2 A}{2(g \pm x) + {}^{l_c}/_{\mu_r}} \tag{2.4}$$

It can thus be seen that the inductance of the actuator is inversely proportional to rotor position. Substituting (2.4) into (2.1) provides the coil current equation.

$$\frac{di}{dt} = \frac{2(g \pm x) + {}^{l_c}/_{\mu_r}}{\mu_0 N^2 A}(v - iR) \tag{2.5}$$

From (2.5) it can be seen that variation of the current in the coil is proportional to the movement of the rotor.

2.1.2 Amplitude modulation approach

Amplitude modulation is a technique used to obtain the position information from the switching power amplifier outputs. The current signal contains the position information and the voltage signal contains the duty cycle variations of the power amplifier.

Signal processing in the digital domain provide a number of advantages that will be discussed further in Section 2.2.1. Because of these advantages, self-sensing techniques can be implemented both in the analogue and digital domain, or can be implemented exclusively in the digital domain.

Figure 2.4 illustrates the amplitude modulation based on the work of Schammass [3] for one degree of freedom on the AMB. To explain the self-sensing technique further, a few waveforms will be shown at various stages of the demodulation process.

Figure 2.5 shows the position of the AMB's rotor with a sinusoidal disturbance. It should be noted that this signal is not the actual measurement of an AMB's rotor position but only a generated signal for illustration purposes.

A modulated current through a coil of the AMB, under ideal circumstances, is shown in Figure 2.6. The carrier frequency is the switching frequency of the power amplifier, and the modulation component is the changing inductance due to the change in rotor position.

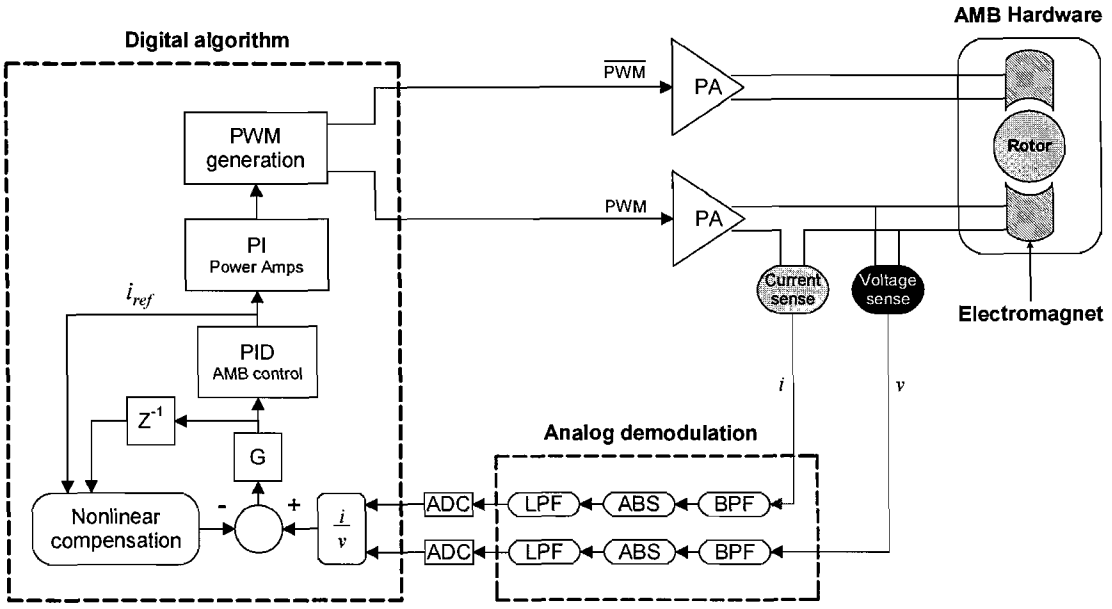


Figure 2.4: Amplitude modulation self sensing

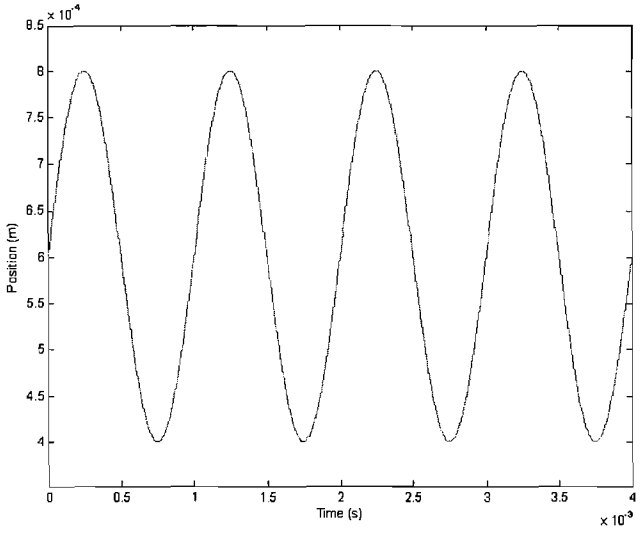


Figure 2.5: Actual position of rotor

In the system the modulated current will be sensed by a current sensor and passed through a band pass filter (BPF). The BPF produces the fundamental components of the current and voltage signals. Illustrated in Figure 2.7 is the band pass filtered current signal.

The absolute (ABS) value of the signal is obtained and low pass filtered (LPF) to produce the envelope of the signal. The envelope of the current signal can be seen in Figure 2.8. Only low sampling ADCs is necessary for digitizing the envelope components because they will be no higher than 500 Hz, which is the bandwidth of the AMB.

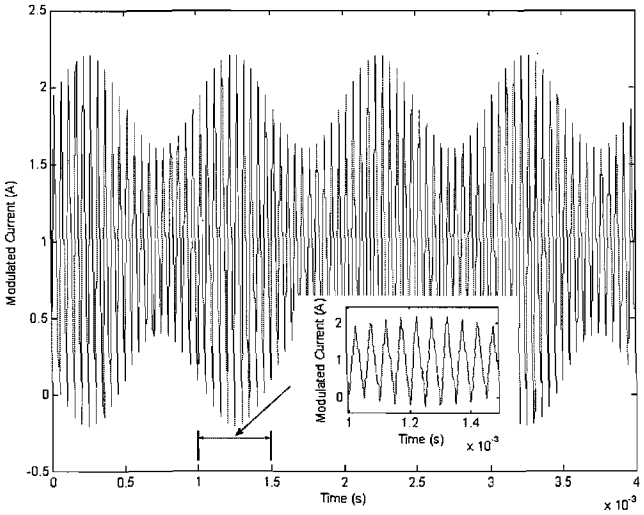


Figure 2.6: Modulated current

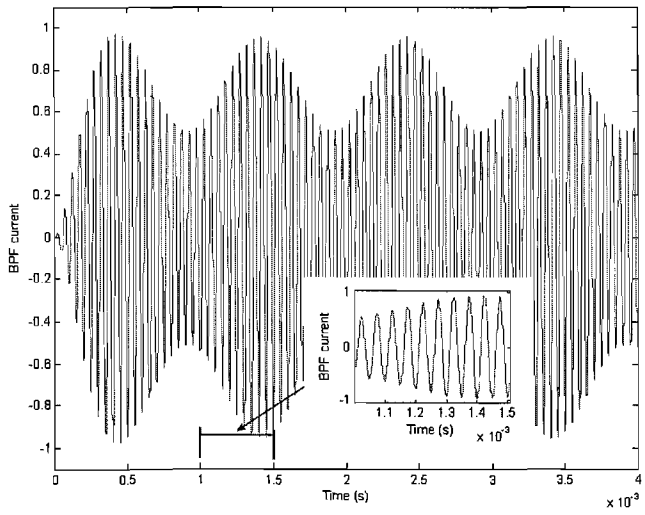


Figure 2.7: Current after band pass filter

In the digital domain the demodulated current is divided by the demodulated voltage to compensate for duty cycle changes. The output of the division is already an estimation of the rotor position but is unscaled and contains no compensation for non-linear effects. The non-linear effects are caused by, for instance, the B-H curve of the magnetic material used in the electromagnets. The self-sensing algorithm needs to compensate for nonlinear material effects. This is done by using one delayed position estimation and the reference current. Further details on this compensation algorithm is beyond the scope of this thesis.

Other strategies may be implemented for demodulating the current and voltage signals. For

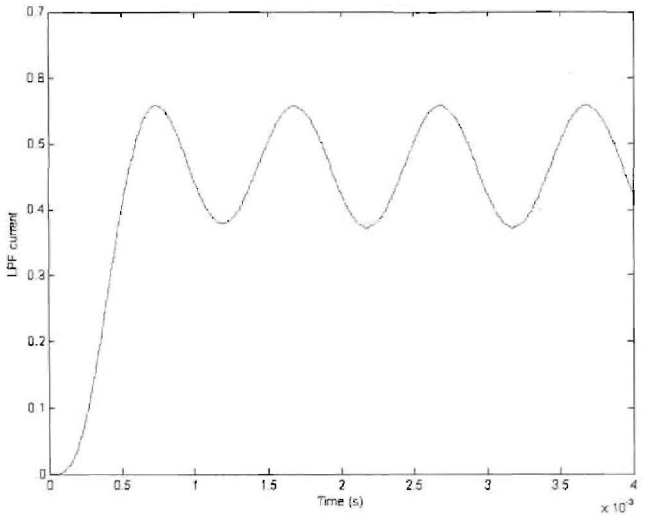


Figure 2.8: Current after low passed filter

instance, directly after analogue band pass filtering, the high frequency signal can be sampled by a high sampling ADC, typically in the range of 1 Msps. This high sampling rate will ensure proper representation of the 20 kHz signal in the digital domain. Sampling a 20 kHz signal at 1Msps will result in having 50 data points for every 50 µs time period.

After sampling a processor can perform a fast fourier transform (FFT) on the signal and obtain the peak amplitude value of the FFT. The peak value is used for estimating the rotor position. This technique is illustrated in Figure 2.9 which shows only the current demodulation. Voltage demodulation is performed in exactly the same manner.

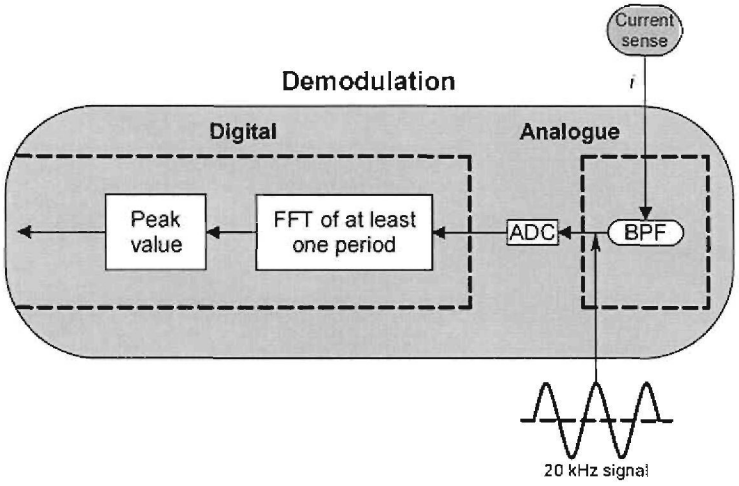


Figure 2.9: Demodulation using an FFT

Another possible technique is illustrated in Figure 2.10. For this technique the ADC needs to sample exactly on the peaks of the fundamental frequency voltage and current signals. The peak values can again be used for a rotor position estimation.

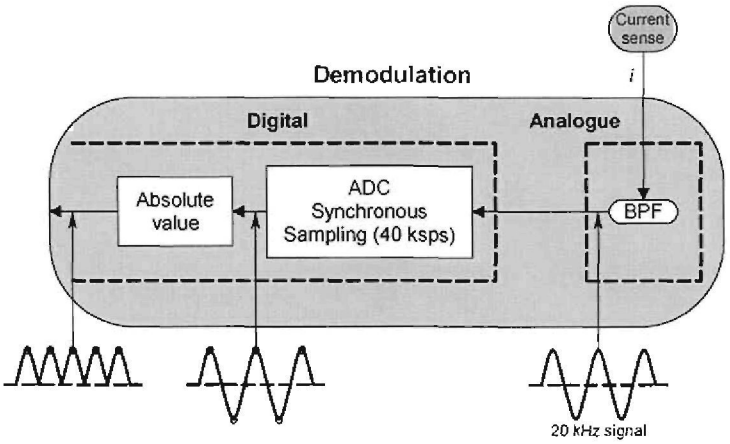


Figure 2.10: Demodulation using synchronous sampling

Some of the techniques requires less digital processing than others. The FFT technique will for instance require a lot more processing resources than the simple analogue modulation technique. All of the techniques can also be fully implemented in the digital domain. In order to adequately investigate different self-sensing techniques a powerful processor is required that offers flexibility and performance.

2.2 Processors

Digital signal processing (DSP) has become a indispensable part of industrial applications such as telecommunications, digital television, digital audio, instrumentation and cellular phones to name just a few. DSP architectures are becoming cheaper and more commonly available, and thus poses more attractive design solutions for signal conditioning applications [9].

The designer of a system is often faced with a choice between analogue signal conditioning and DSP. Because of the many advantages of DSP, as will be discussed in section 2.2.1, it might be more appealing to perform signal conditioning in the digital domain. A variety of architectures are available to the designer for implementing DSP. In the following sections (2.2.1 and 2.2.2) two possible architectural choices will be discussed: Digital Signal Processors (DSPs) and Field Programmable Gate Arrays (FPGAs).

2.2.1 Digital signal processors (DSP)

Digital signal processors (DSPs) contain specialized architecture that enables it to be much more efficient at digital signal processing than general purpose processors (GPP) [10].

Advantages - DSP offers some significant advantages over analogue signal conditioning. Some of these advantages include [9],[10]:

- Digital signals can be sent over large distances without losing data;
- Using analogue components to filter signals is expensive and requires fixed detailed design of components. Digital filtering is flexible in the sense that the programmed code can be reconfigured;
- Perfect copies can be made of digital signals where copied analogue signals decay with each copy;
- Performance of the digital processor doesn't change with temperature or age;
- DSPs can be used to perform functions not possible with analogue signal processing.

Disadvantages - As with any engineering application, DSP has some drawbacks that needs to be weighed against the advantages [9]:

- Speed and cost: DSPs can be expensive, especially when large bandwidth is a requirement. Analogue to digital converters (ADCs) and Digital to Analogue Converters (DACs) are either too expensive or cannot provide enough resolution for high bandwidth DSP. DSPs are only fast enough to process signal with a moderate bandwidth. Analogue processing is still used for signals in the 100 MHz range.
- Design time: Without the necessary resources and sufficient knowledge in DSP techniques, DSP design can be very difficult and time consuming.
- Finite word length: The amount of bits used to represent data should be carefully chosen as not to degrade system performance.

Design considerations

Before any design can be initiated the requirements of the user need to be determined and a list of design constraints should to be drawn up. Some important characteristics to consider when choosing a digital signal processor are the following [9],[10]:

Programmability - The end product may either be application specific or general purpose (programmable). Programmable devices are more flexible and the developers can then easily change functionality for specific needs.

Throughput - Some applications need data to be processed and outputted faster than in other applications. For example high definition TV (HDTV) needs decoding in the Mega bits per second range (Mbps) where motor control only need a bit rate in the thousands of bits per second (kbps) range.

On-chip memory - The amount of on-chip memory significantly influences the physical silicon size of a chip, and thus also the price. The advantages of on-chip memory are also worth mentioning though:

- Eliminates need for external memory and reduces board space;
- Access performance is increased and thus also overall throughput performance;
- Lower power consumption.

Integration - Processors may have a variety of on-chip peripherals, reducing the need for external devices. A variety of options are available and should be considered by the designer.

Power - Power dissipation will be more crucial in handheld devices than devices that plug into a power outlet such as a wall socket. Chips that consume less power are more expensive but might be worth considering in certain applications.

Real-time responsiveness - "Real-time" refers to the ability to perform a task within a limited time frame. Different processors operate at different speeds and it is up to the designer to decide if the processor will meet the real-time constraints. The speed of a processor is typically measured in Million Instructions Per Second (MIPS).

Type of arithmetic - Floating point and fixed point arithmetic are typically used in DSPs. Floating point arithmetic represents numbers in the form of a mantissa and an exponent value, and is used in applications with a wide dynamic range. The dynamic ranges of signals differ in each application. Dynamic range can be considered as the difference in the largest and smallest value of a signal to be represented. Fixed point arithmetic represents only integer values, and is used in cheaper, high volume applications.

Word length - The higher the word length the more accurately signals can be represented in the digital domain. Simplistically one may conclude that higher word lengths will result in for example better audio quality, but will require more resources (memory, MIPS) from the DSP.

Standards - Standards often specify certain performance requirements that must be taken into account when designing a system.

High availability - In some applications availability is crucial. For example if a telephony system crashes, replacement parts need to be available.

DSP on-chip technology

As mentioned in the first paragraph of Section 2.2.1 a DSP has a specific architecture that increases its performance when executing DSP functions. Some built in technologies that make this possible include the following [9],[10]:

Multiply and accumulate unit (MAC) - Signal processing involves a great deal of multiplication, when considering for instance (2.6).

$$result = x_1 * c_1 + x_2 * c_2 + x_3 * c_3 + ...x_n * c_n \tag{2.6}$$

A DSP has built in architecture that can perform the multiplication of two numbers and the adding of the result to all previous multiplications, in one clock cycle.

Pipelining - An instruction can be broken down into three steps, that is instruction fetch, decode and execute.

Figure 2.11(a) illustrates that with overlapping a new instruction can be started every clock cycle.

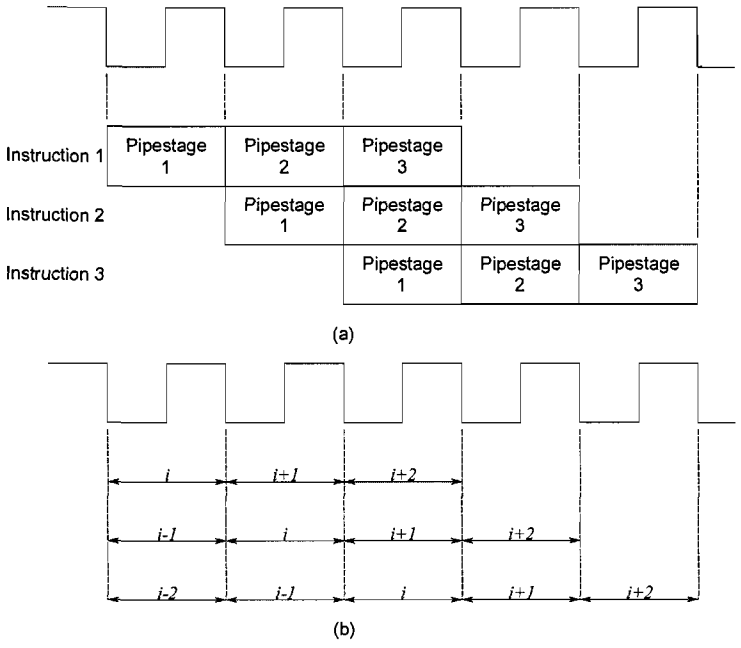


Figure 2.11: Illustration of pipelining [9]

In Figure 2.11(b) one can see that three operations can be executed simultaneously:

- the i^{th} instruction is fetched;
- (i-1) th instruction is decoded;
- (i-2) th instruction is executed.

Code density with very long instruction words (VLIW) - VLIW is an instruction that represents several operations executed at the same time by the DSP.

Harvard architecture - The Harvard architecture specifies memory where data and code lie in separate spaces. This enables the DSP to simultaneously fetch the next instruction and execute the current instruction.

Zero overhead looping - Typical DSP algorithms have what is known as a critical loop. An algorithm, for example voice decoding, is executed many times within a loop. Loop management in GPPs requires many clock cycles. In DSPs a special architecture manages the loop. The result is that the management of the critical loop requires zero clock cycles.

Circular buffers - In functions such as Finite Impulse Response (FIR) filters, memory of previous values are required. Developers use a circular buffer to implement the delay line (list of previous values) efficiently. This involves re-using a small block of memory and wrapping back to the top if the bottom is reached. In DSPs built-in architecture can manage circular buffers and eliminate extra overhead processing.

DSP technology, if correctly implemented, may greatly improve the efficiency of processing digital signals. Although DSP offers some degree of simultaneous processing with pipelining technology, it still lacks true parallelism. Field programmable gate arrays (FPGAs) can perform a large number of instructions every clock cycle.

2.2.2 Field programmable gate array (FPGA)

A microprocessor has a fixed hardware architecture and runs a program. In the case of an FPGA, the programmability is intended at the hardware level. The code implemented on an FPGA is thus used to reconfigure the hardware setup of an FPGA [11].

The basic architecture of an FPGA is based on configurable logic blocks (CLBs) with programmable interconnects or switch matrices. Figure 2.12 illustrates a block architecture of a FPGA with the following basic components[11],[12]:

Configurable logic block (CLB) - The CLB is the basic logic unit of an FPGA that constitutes a reconfigurable switch matrix with 4 or 6 inputs, selection circuitry (Multiplexer, etc) and flip-flops. The switch matrix can be configured to manage RAM, combinational logic or shift registers.

Interconnect - Flexible interconnections provide routing of signals between CLBs, and also routes signals to/from the Inputs/Outputs (I/Os).

SelectI/O - Modern FPGAs provide a wide variety of I/O standards allowing the designer to select the ideal system interface. I/Os are arranged in banks, each bank providing different I/O standards for interfacing.

Memory - Embedded block memory enables the designer to include on-chip memory in designs.

Complete clock management - Xilinx FPGAs have build in digital clock managers that reduce jitter and phase-locked loops for clock synthesis.

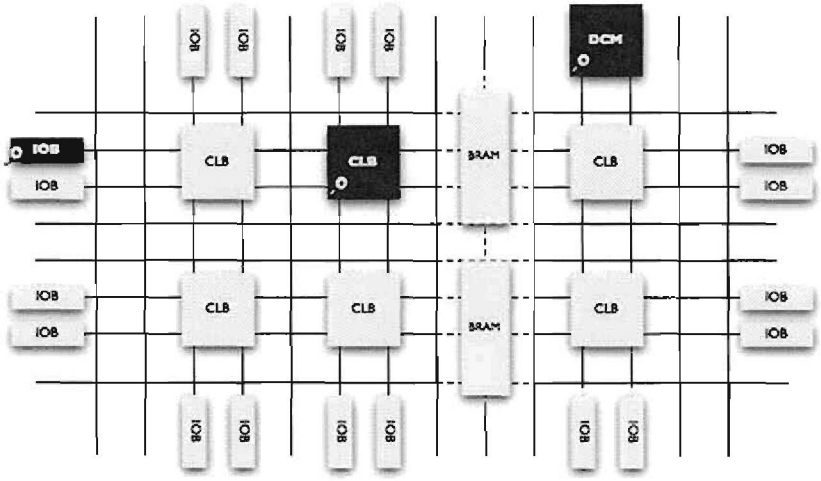


Figure 2.12: FPGA structure [12]

VHDL

The acronym VHDL stands for VHSIC Hardware Descriptive Language, where VHSIC is the abbreviation for Very High Speed Integrated Circuits. The application of VHDL includes the programming of FPGAs, Configurable Logic Devices (CPLDs) and Application Specific Integrated Circuits (ASICs) [11].

The execution of VHDL statements are inherently parallel. For this reason VHDL is referred to as code rather than a program. Statements can be placed inside certain keyword program blocks such as PROCESS, FUNCTION or PROCEDURE that will force the code to be executed sequentially [11].

Figure 2.13 illustrates a simplified design flow of VHDL code. A design specification is drawn up that specifies how the final design is required to behave.

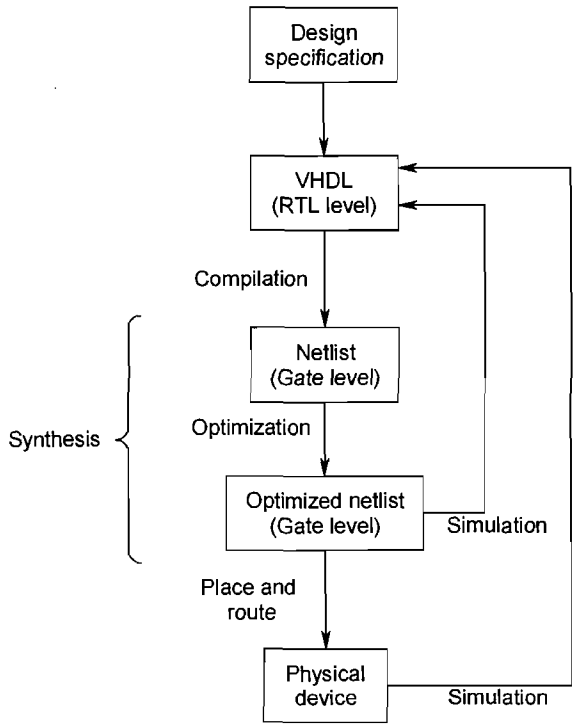


Figure 2.13: VHDL design flow summery [11][13]

A register transfer level (RTL) description is created which is basically the VHDL code. An editor is used for creating the VHDL code and saved with the extension .vhd. The code is synthesized into a netlist which is descriptive of the RTL at gate level and can be optimized for either speed or area [11],[13].

Simulations are run next which is an important part of the design process. The designer uses the simulations to verify the design. If simulation results are unsatisfactory, the VHDL needs to be edited and re-synthesized [11],[13].

Place and route software is used to generate the physical layout on a target device such as an FPGA. Place and route does the following [13]:

- The netlist's basic functions (primitives) are placed into an appropriate location on the target device.
- Signals are routed between the primitives according to the netlist design.

Post route simulation is the final verification process before the device is programmed. Post route simulation checks whether the place and route process was successful by verifying that the design will meet the specified constraints (for example timing constraints). The post route simulation is run after the place and route process has been executed [13].

Summary

Digital Signal Processors might have architectures specifically designed for DSP based operations, but might still suffer to meet demanding real time constraints. The FPGA offers high speed processing of algorithms that would benefit from parallelism, such as FFTs and FIR filters. Implementing the FPGA as a co-processor to the DSP will greatly increase performance and yield a very powerful hardware system capable of processing complex algorithms in real time [14],[15].

2.2.3 Co-processing

In many applications only 20 % of the code on a DSP will use up 80 % of its processing power (MIPS). This 20 % represents the core algorithms in the application. The other 80 % of the code is responsible for execution control and initialization. The designer is faced with reducing the processing load of the 20 % along with trying to limit the complexity of the remaining 80 % [15].

A co-processor is ideal in this situation for offloading some of the load caused by the power hungry 20 % code. The designer must now determine exactly what is to be offloaded to the co-processor [15].

For this the designer can use the development tools of the DSP. Texas Instruments' Code Composer Studio (CCS) provide profiling functions that can be used to indicate the amount of resources a particular function is consuming. Some criteria by which to consider the algorithms to be offloaded are [15]:

- The algorithms should at least be responsible for half of the processor load;
- Clustered algorithms, that are only dependent on onr another's outputs, will limit the co-processors dependency on the DSP. The DSP only has to send data for the co-processor and receive the result without having to interfere with the co-processor's operations.
- Implementing the algorithms should be easily implementable on the hardware and have a repetitive structure.

The interface between the DSP and co-processor is dependent on the peripheral hardware on the DSP. For Texas Instrament's DSPs, possible options include 16/32/64-bit Extended Memory Interface (EMIF) and Multichannel Buffered Serial Ports (McBSP) [15].

2.3 Communication

Consider an AMB controller system such as the one depicted in Figure 1.3. The system constitutes a main controller and several slave controllers. Some form of data transfer link is required between the main and slave controllers. Data transfer is also necessary for data logging and analysis. This might imply a convenient interface link to a PC such as a USB or RS232 connection. The next three sections discuss three industry standard interface protocols that are frequently used in a wide variety of applications. They are: Controller Area Network (CAN), RS232 and RS485.

2.3.1 CAN bus

The Controller Area Network (CAN) bus architecture was originally developed for use in cars to replace complex wiring systems. It is a robust protocol that has the ability to self diagnose and repair data errors. The protocol specifies a 2-wire differential signal on the physical level and thus gives the CAN-bus excellent noise immunity. Figure 2.14 displays a typical CAN bus. The CAN bus can support up to 30 nodes on the bus [5],[16].

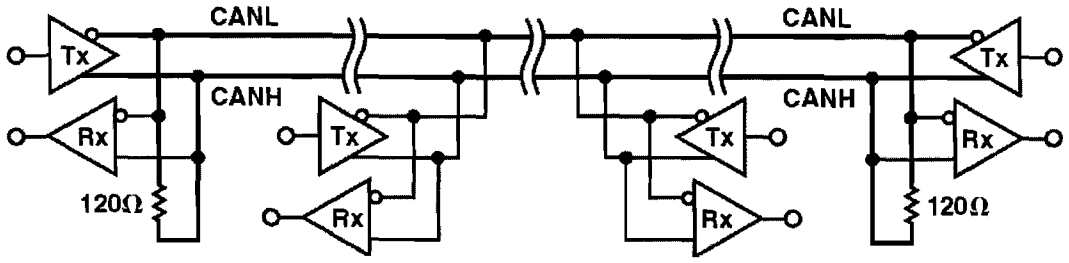


Figure 2.14: CAN bus [5]

The CAN bus driver produces a differential signal that constitutes high and low voltage, that is placed on the CANH and the CANL signal wires respectively. Together the high and low voltages form the dominant signal on the bus that represents a logic low. When no node/transmitter is transmitting, pull up resistors drive the bus to Vcc/2, where Vcc is the supplied voltage to the transmitter. This is the recessive signal level and represents a logic high. Figure 2.15 illustrates these levels. In the dominant state, CANH is typically (Vcc-0.9 V) and CANL is 1.5 V [5],[16].

Table 2.1 summarises the CAN bus specifications.

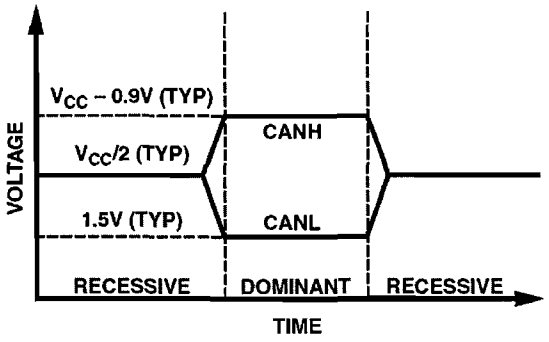


Figure 2.15: CAN bus signals [5]

Table 2.1: CAN bus specifications

Max Speed	Max Distance	Transmission	Signal	Multipoint	Robustness
1 Mbps	40 m	Asynchronous	Differential	Yes	High

2.3.2 RS232

RS232 is not a very fast or reliable communication protocol but is easy to design and implement. The RS232 driver produces a large drive voltage of ±(5 to 15 V). The receiver is triggered by signals above 3 V or below -3 V and are unbalanced. This implies that the signal levels are referred to ground. A logic 0 will be detected if the signal is above 3 V relative to ground and a logic 1 will be detected when the signal is below -3 V relative to ground [16],[4]. A RS232 bus and its signal levels are illustrated in Figure 2.16.

The RS232 protocol specifies some control signals in addition to the data signals. These control signal may or may not be used in the communication setup. They are the following:

- DCD - Data carrier detect
- DSR - Data set ready
- RTS - Request to send
- CTS - Clear to send
- DTR - Data terminal ready
- RI - Ring indicator

Summarised in table 2.2 is the RS232 specifications.

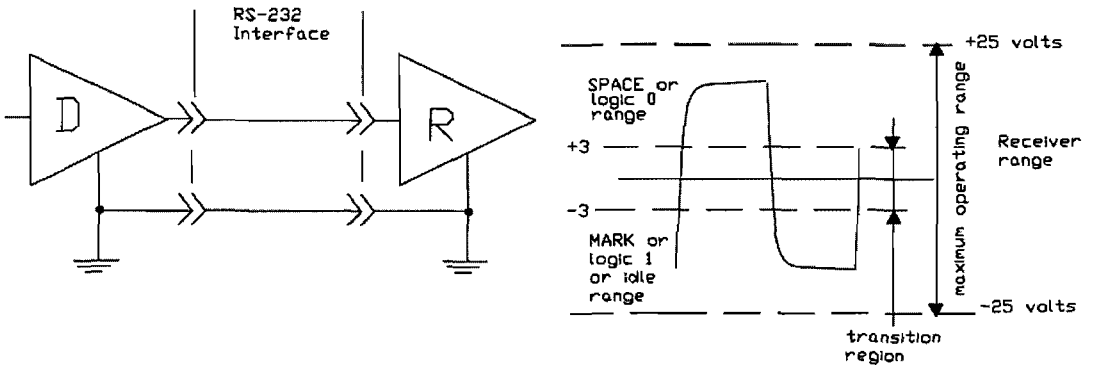


Figure 2.16: RS232 bus [4]

Table 2.2: RS232 specifications

Max Speed	Max Distance	Transmission	Signal	Multipoint	Robustness
1 Mbps	20 m	Asynchronous	Unbalanced	No	Low

2.3.3 RS485

RS485 supports multipoint architecture, which implies that there can be multiple drivers interfaced with multiple receivers. These interfaces specify balanced data transmission schemes. This makes the interface robust and capable of operating in noisy environments [17].

The voltages used for logic levels appear across a pair of signal lines that transmit only one signal. The terminals of the receiver and its connector does have a ground connection but the logic level is not referred to this ground [4].

The logic states are defined as follows [4]:

- When the voltage on terminal A of Figure 2.17 is negative with respect to the voltage on terminal B, a logic 1 will appear on the output of the receiver.
- When terminal A is positive with respect to terminal B, the line is a logic 0.

Differential receiver

The RS485 receiver can tolerate a maximum common mode voltage (Vcm) of -7 V/+12 V. The common mode voltage is defined as the mean voltage of terminals A and B with respect to signal ground. If the differential input voltage (V) is greater than 200 mV, a logic state will appear on the output of the receiver. When the differential voltage is less than -200mV, the inverse logic state will appear on the output of the receiver [4][17].

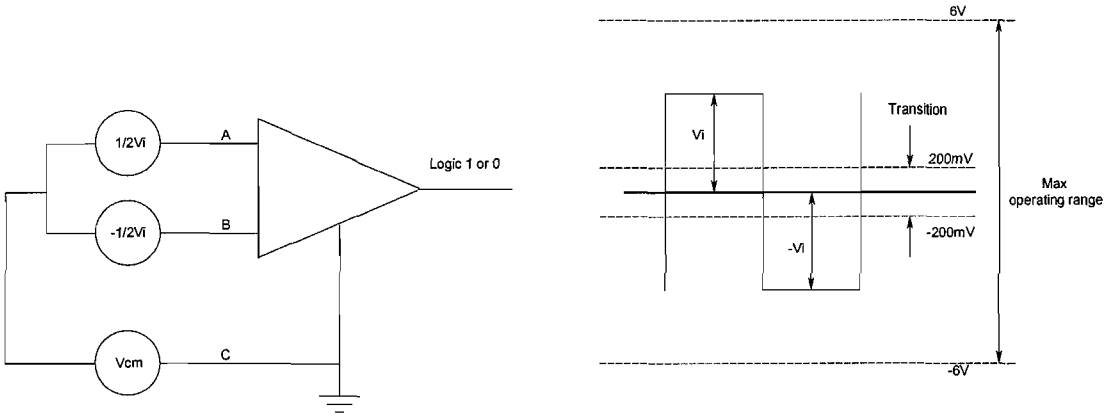


Figure 2.17: RS485 receiver and signal levels

Differential transmitter

The differential voltage V_{AB} generated will stay inside hte ranges 1.5 V to 6 V and -6 V to -1.5 V as illustrated in Figure 2.18.

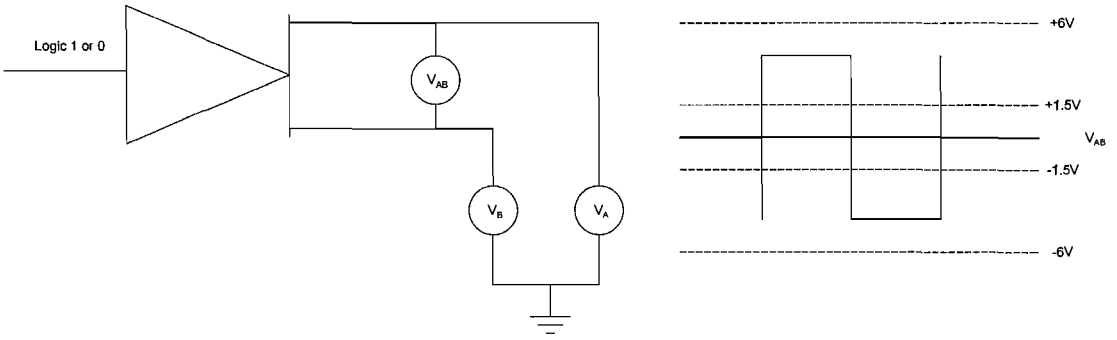


Figure 2.18: RS485 transmitter and signal levels

Figure 2.19 shows a typical multidrop RS485 network. The enable line is used to enable or disable the driver. A logic 1 enables the driver and a 0 disables the driver. When the driver is disabled, it is put into the tristate condition. This effectively disconnects the driver from the line and is necessary to permit other drivers to send data over the same transmission line. If two drivers try to transmit data at the same time, erroneous data might occur. This is called line contention.

RS485 specifications can be summarised in table 2.3.

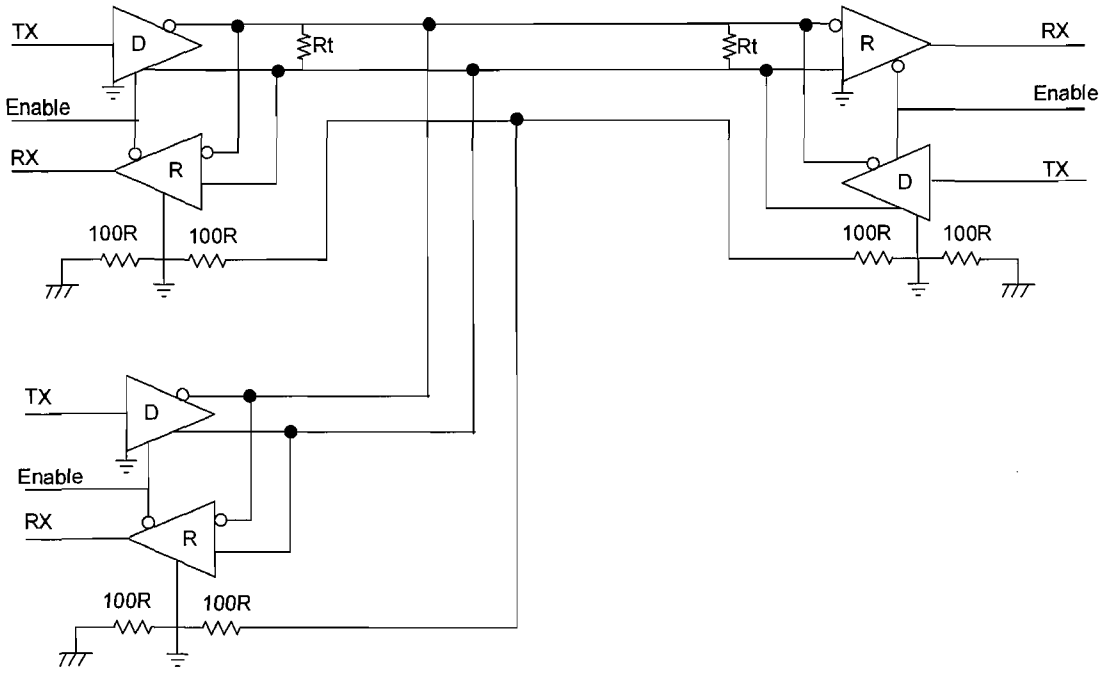


Figure 2.19: RS485 bus

Table 2.3: RS485 specifications

Max Speed	Max Distance	Transmission	Signal	Multipoint	Robustness
20 Mbps	1.2 km	Asynchronous	Differential	Yes	High

2.4 Systems Engineering

Because systems engineering is such a loose term it is appropriate to start off with a description of a few concepts. The general definition for a system as adapted from [18] is:

An assemblage or combination of things or parts forming a complex or unitary whole: a mountain system or a railroad system; any assemblage or set of correlated members: a system of currency; an ordered and comprehensive assemblage of facts, principles, doctrines, or the like in a particular field of knowledge or thought: a system of philosophy; a coordinated body of methods or a scheme or plan of procedure: a system of government; any formulated, regular, or special method or plan of procedure: a system of marking, numbering, or measuring; the world or universe.

For the purpose of this section it is necessary to narrow the definition of a system down to an engineered system. Some recognizable traits of an engineered system can be summed up as follows [19]:

- "Engineered systems have a *functional purpose* in response to an identified need and have the ability to achieve some stated *operational objective.*
- Engineered systems are *brought into being* and *operate* over a life cycle, beginning with a need and ending with a phase out and disposal.
- Engineered systems comprise a *combination of resources*, such as humans, information, software, materials, equipment, facilities, and money.
- Engineered systems comprise of *subsystems* and related *components* that *interact* with one another to produce the systems response or behaviour.
- Engineered systems are part of a *hierarchy* and are influenced by external factors from larger systems of which they are a part.
- Engineered systems are *embedded* into the natural world and *interact* with it in desirable as well as undesirable ways."

The product might be considered only a part of a complete system, for instance the engine of an automobile. A product might also be the system itself, for example an air traffic control system that converts air traffic mayhem into an organized flow. Consumable products include bread, lubricants, batteries, solder paste, anything that cannot be repaired. Repairable products, e.g. forklift, guidance system or machine tools are often called *prime equipment* when it serves a larger system purpose.

Classical engineering is more concerned with the final product's performance than with the process of developing the product. It tries to find the most economical way, with the least resources, to develop a product that will improve the lives of people [19].

No product can come into existence without a development and construction process, and cannot keep functioning without maintenance and support. Systems engineering may be considered as the management of all aspects in the life cycle of a system. No one formal definition exists for systems engineering, and is more dependent on an individual's experience or the organization wherein it is used. The following are two published definitions [19]:

"An interdisciplinary approach encompassing the entire technical effort to evolve into and verify an integrated and life-cycle balanced set of system people, product, and process solutions that satisfy customer needs. Systems engineering encompasses (a) the technical efforts related to the development, manufacturing, verification, deployment, operations, support, disposal of, and user training for, system products and processes; (b) the definition and management of the system; (c) the translation of the system definition into work breakdown structures; and (d) development of information for management decision making." [20]

"An interdisciplinary collaborative approach to derive, evolve, and verify a life cycle balanced system solution which satisfies customer expectations and meets public acceptability." [21]

The following sections discuss some system engineering concepts that is adapted from [19].

2.4.1 System life-cycle

It is important to understand the life cycle of a system in order to apply system engineering concepts. The product life cycle, as illustrated in Figure 2.20, starts at a need, followed by a conceptual design, detail design, production and finally product use and disposal.

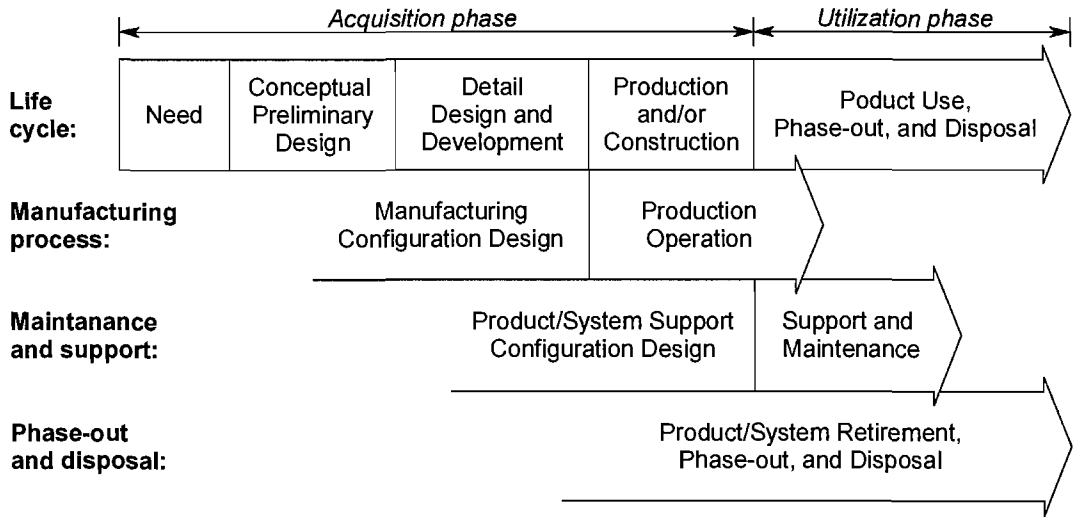


Figure 2.20: Product and system life cycles [19]

Some of the system's life cycles that are often neglected, but equally important, are the manufacturing, maintenance and support, and product retirement. These life cycles should run in parallel with the product life cycle. The design of the system should not just focus on the product itself but should also consider operational outcomes that include producibility, reliability, maintainability, usability, supportability, serviceability and disposability.

2.4.2 System specification

In the conceptional design phase of a system life cycle, it is necessary to specify an overall guideline for system design. This top level *system specification*, also referred to as a Type A specification, will provide a baseline for development of lower level specifications: *development* (Type B), *product* (Type C), *process* (Type D) and *material* specifications (Type E).

A Type A specification includes the resulting specifications obtained from activities such as a *system feasibility analysis, system operational requirements, maintenance and support concept, technical performance measures* and *functional analysis and allocation.*

System feasibility analysis

After having identified a need for a system, it is necessary to explore various design approaches. The approaches should be evaluated and the most feasible one identified in terms of performance, effectiveness, difficulty of design and production, maintainability, cost and other resources that will be required.

System operational requirements

The next step after having decided on the design approach, operational scenarios need to be identified. Questions to ask are: "What are the anticipated type and quantities of equipment, software, personnel, facilities, etc., required, and where are they to be located? How is the system to be utilized, and for how long? What is the anticipated environment at each operational site? How is the system to be supported and for how long?" [19] By answering these questions the operational requirements for the system can be set up.

Maintenance and support concept

The maintenance part of the system is often neglected in the design phases as a result of the focus only being on the performance of the system. The system and its elements should be designed in such manner that they can be effectively maintained throughout their life cycle. Maintenance can be preventative and/or corrective.

Technical performance measures

Technical performance measures (TPMs) refer to the quantification of the system's performance such as range, accuracy, bits, capacity, processing time, speed, etc. Other performance factors include mean time between maintenance (MTBM) and failure rate. There may be many TPMs specified for a system to ensure that the system will meet the customer's needs effectively and efficiently.

Functional analysis and allocation

In the preliminary and conceptual design phase a functional description of the system will serve as a way to determine the necessary resources required for the system to fulfil its purpose. A *function* can be described as the action that needs to be performed in order to achieve a specific goal. Defining the functions of a system focuses on the *whats* and not the *hows* (What is to be accomplished, not thinking about the how at this stage).

Functional flow block diagrams (FFBDs) can be used to encompass the functional analysis of a system. A top level functional flow can be broken down into a second, third level etc. functions, down to the necessary level to describe the system and all its elements. The blocks are numbered (see section 3.2) to show relationships and for traceability. Traceability refers to the top-down link between the requirements and the functional analysis and the bottom-up link of the resources necessary to perform the functions. This way the requirements and resources can be referred back to a function, justifying the resources and ensuring the system meets all the requirements.

The next step is to partition the system and allocate resources to the partitioned elements. A group of functions closely related should be assigned a common resource in order to accomplish multiple functions if possible.

The system's architecture should have become more apparent after system partitioning. System architecture is a top level representation of the structure of the system and its interfaces. It can be derived from the functional analysis making it the functional architecture. From the functional architecture the physical architecture can be derived, evolving the *whats* into *hows*.

2.4.3 Conclusion

The specification constitute an important part of the system engineering process. In Chapter 3 to follow an adapted version of the integrated controller's specification is presented to the reader. The original specification is fully presented in Appendix A.

Chapter 3

System specification

Chapter 3 will specify the integrated controller in terms of functional units, functional architecture, functional units with performance specifications and mechanical constraints. These specifications provided a baseline for the development of the integrated controller.

3.0.4 Introduction

Although off the shelf systems, such as single board computers (SBCs), are available that incorporates powerful processors, ADCs and various communication interfaces, they all have one or the other shortcoming for the purpose of investigating self-sensing techniques. Before analogue signals are digitized by an ADC, they usually need some form of conditioning such as buffering, filtering and/or scaling. Analogue circuitry is required for this and will need to be added externally to an SBC. The same goes for power electronics. If the SBC needs to drive a switching power supply, the power electronics will require an external add-on.

It was regarded feasible to develop a custom integrated controller that would incorporate analogue, digital and power electronics. The integrated controller's purpose would be aimed mainly to investigate and implement self-sensing techniques, but still be generic enough for alternative applications such as driving a motor or controlling an AMB system by traditional means, using expensive position sensors.

A project management plan had to be drawn up to ensure proper coordination of the development process for such a complex system. A specification was generated to define the following:

- Functional architectural units;
- Interfaces between units;

- System functionality and performance specifications;
- Resource allocation (who designs what);
- Physical constraints.

3.1 Integrated controller functional architecture

The following sections will break down and describe the architectural units for the integrated controller. Three top level architectural sections was identified: Analogue circuitry, Digital Circuitry and Power Electronics.

3.1.1 System functional architecture

Figure 3.1 shows the block representation of the integrated controller system architecture. This is the top level view of the complete system to be developed.

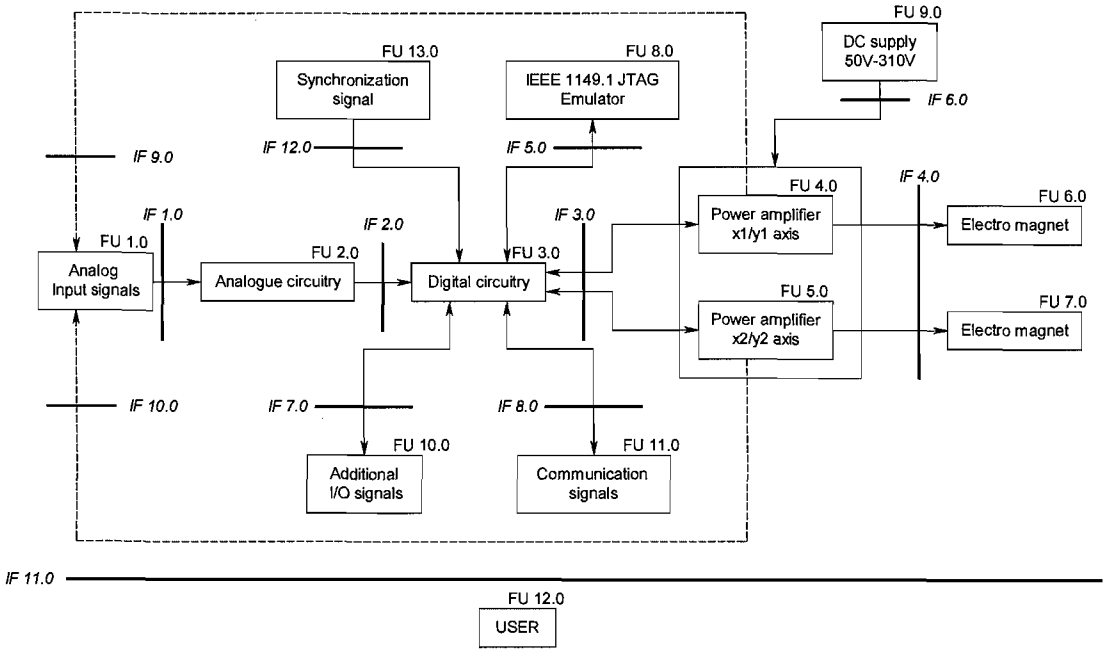


Figure 3.1: Functional unit architecture of the integrated controller

Functional Units are labelled FU x.x and the interfaces are labelled IF x.x. The numbered labelling allows for ease of referencing and matching detail designed objects with the specification. Each numbered unit in the architectural design will now be discussed briefly.

Functional Unit 1.0: Input signals - The integrated controller need to be able to support the input of certain analogue input signals. Table 3.1 lists these signals. It is seen in the table that an embedded device and a co-processor is mentioned. Texas Instrument's TMS320F2812 DSP will be used for the referred main embedded device and a Xilinx Spartan 3E XC3S500E FPGA will be implemented as the co-processor. The motivation for the choices in embedded devices is discussed in Chapter 4.

Table 3.1: Analogue input signals to integrated controller

Number of inputs	**Type**	**Range**	**Input to:**	**Signal obtained from**	**Bandwidth**
1	Position signals	0 to -24 V	Main Embedded device	External	0 to 2 kHz
3	Additional external signals	N/A	Main Embedded device	External	0 to 2 kHz
2	Power Amplifier current sense	Depends on sensor to be used	Main Embedded device	Power Amplifier	0 to 2 kHz
4	Sense circuitry	$\pm$10 V	Co-processor	Power Amplifier	0 to 500 kHz

Position signals - Eddy current sensors are typically used to determine the rotor position of the AMB. These sensors produce analogue output signals proportional to the position of the rotor relative to the sensing point.

Additional external signals - The design should facilitate the option for additional analogue signals not currently specified. This will provide the option of future expansion and broaden the integrated controller's generic functionality.

Power Amplifier current sense signals - A current sensor will sense the current through the load of the Power Amplifiers (PAs) to enable PA closed loop control.

Sensing circuitry signals - The current and voltage output of the PAs will be conditioned in an attempt to extract the position of the rotor from the signals without using expensive eddy current sensors.

Functional Unit 2.0: Analogue Circuitry - The analogue circuitry has the purpose of conditioning all incoming analogue signals. After analogue conditioning the signals will be digitized and used in algorithms executed by embedded processors.

Functional Unit 3.0: Digital Circuitry - This block represents all circuits and components that will process the digital signals in the design.

Functional Unit 4.0 and 5.0: Power Amplifiers - The system will include two 3-phase power amplifiers.

Functional Unit 6.0 and 7.0: Electro magnets - These blocks are representative of the AMBs' electromagnets that the integrated controller will be driving. The electromagnets are not included in the design.

Functional Units 8.0: IEEE 1149.1 JTAG emulator - A JTAG emulator will be used to program embedded processors included in this design.

Functional Unit 9.0: DC SUPPLY 50 V-310 V - The integrated controller system will draw its power from a DC input voltage with a range of 50 to 310 V.

Functional Unit 10.0: Additional input/output signals Not all of the pins of the embedded controllers will be used in the design. Provision should be made to allow easy access to the unused pins on a connector for added generic capability.

Functional Unit 11.0: Communication Signals - Communication interfaces will enable multiple integrated controllers to interface with one another and provide data logging functionality.

Functional Unit 12.0: User - The user block indicates that there will be human interfaces; tactile (Switches) and visual (LEDs).

Functional Unit 13.0: Synchronization signal - Synchronizing several integrated controllers that are connected to the same AMB will reduce system noise significantly and increase overall performance.

The analogue, digital, and power blocks will now be broken down into sub architectural blocks.

3.1.2 Analogue circuitry functional architecture

The REF 2.0 block in Figure 3.2 indicates that this is the analogue circuitry's sub-components.

Functional Unit 2.1: Signal conditioning - Analogue signals conditioning will include filtering, buffering and demodulation.

Functional Unit 2.2: Analogue to digital converters (ADCs) - ADCs will be specified in full in section 3.2.

The electronic supply shown in Figure 3.2 is discussed in the following section that describes the sub architectural units of the digital circuitry.

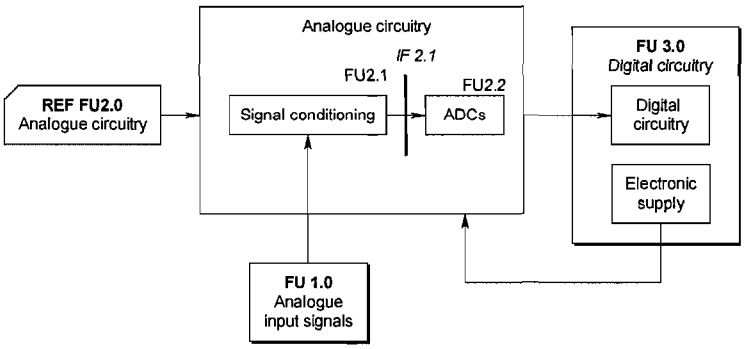


Figure 3.2: Functional unit architecture of the analogue circuitry

3.1.3 Digital circuitry functional architecture

Figure 3.3 shows the digital circuitry broken down.

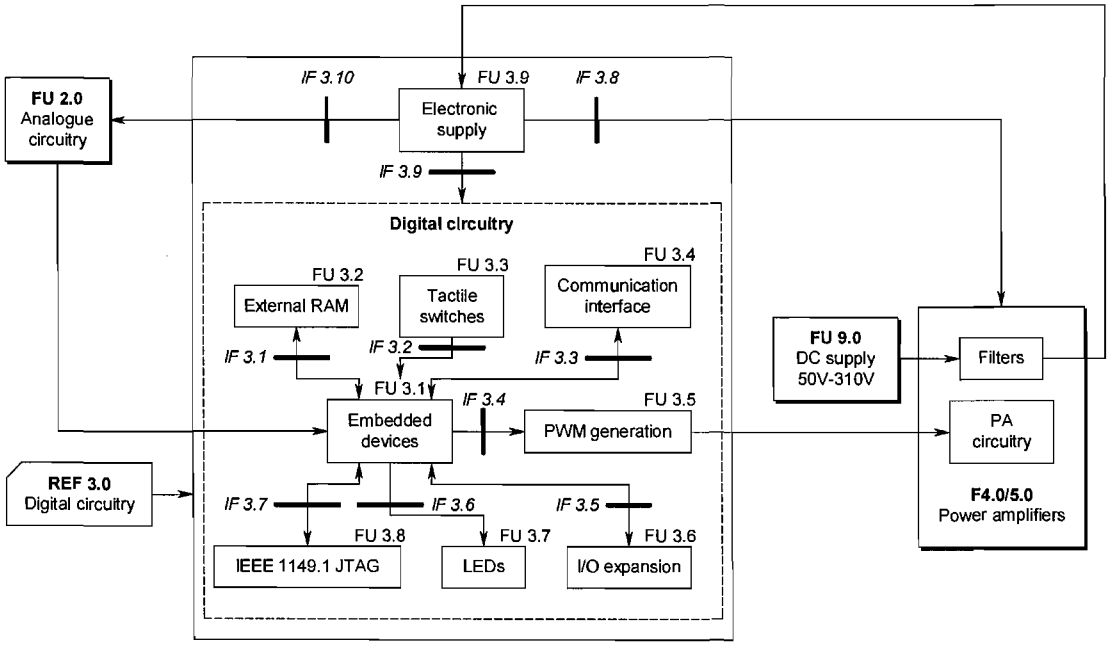


Figure 3.3: Functional unit architecture of the digital circuitry

A description of the blocks labelled FU 3.x is to follow.

Functional Unit 3.1: Embedded devices - In order to gain maximum processing flexibility and power the system will include a processor and co-processor.

Functional Unit 3.2: External RAM - External RAM adds memory for possible use of storing data for analyzing or using it as a general scratch pad area.

Functional Unit 3.3: Tactile switches - Push button switches will give the user an interface to

the integrated controller for manual mode switching or any other possible hard switching that might be required by the user.

Functional Unit 3.4: Communication interfaces - The integrated controller's processors need to be able to send and receive data from off-board sources.

Functional Unit 3.5: PWM generation - This refers to the PWMs that need to be generated for the 3-phase bridges that FU 4.0 and 5.0 refer to.

Functional Unit 3.6: I/O Expansion - The Input/Ouput (I/O) expansion will provide the user with access to processor pins not integrated with a specified purpose in the system design.

Functional Unit 3.7: LEDs - LEDs will give the user a visual interface and prove useful for debugging purposes.

Functional Unit 3.8: IEEE 1149.1 JTAG - A standard JTAG interface will provide an interface for a programming cable that will be used for programming the embedded devices.

Functional Unit 3.9: Electronic supply - The electronic supply or supplies will generate the voltage levels needed for the electronics on the integrated controller. This includes 5 V, 3.3 V 12 V etc. A possible choice for a multi output supply includes a flyback converter [22].

3.1.4 Power amplifier functional architecture

Functional Units 4.0 and 5.0 represent the power amplifiers in the system. An exploded view of the PAs is shown in Figure 3.4. The individual units in the PA architecture is now discussed.

Functional Unit 4.1: Isolation circuitry - A good design practice in PCB layout is to separate the high power electronics and digital electronics [8]. In this case it can be done by placing an optic isolation device between the digital circuitry and the power electronics, and placing the power and digital electronics on different partitions of the PCB. Partitioning can also be accomplished by placing electronics on different PCBs and piggy-backing them on top of each other. Section 3.3 deals with the mechanical requirements of the integrated controller and illustrates the piggy-backing of three separate PCBs.

Functional Unit 4.2: Gate drive circuit - A circuit is required for driving the switching devices that will be used in the 3-phase bridge design.

Functional Unit 4.3: Power circuit: 3-phase bridge - The bridge will have the option of being used either as a three or two phase motor drive. In the case of driving the electromagnets of the AMB it will be used as a 2-phase bridge (H-bridge).

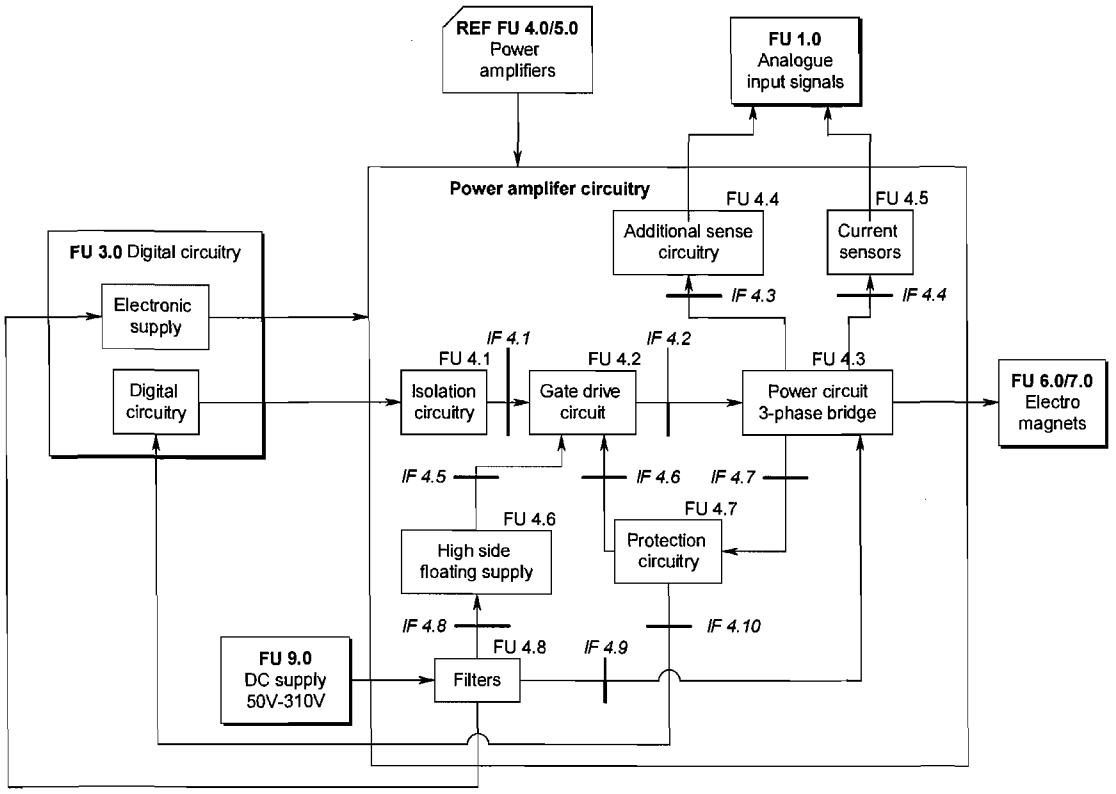


Figure 3.4: Functional unit architecture of the power amplifiers

Functional Unit 4.4: Additional sense circuitry - This function block refers to circuits that will be used to extract the current and voltage signals from the output of the power electronic circuit. These signals can then be used in test algorithms to condition them in such a way that the rotor position might be extracted from them.

Functional Unit 4.5: Current sensors - The current sensors themselves might be included in the additional sense circuitry or function independently.

Functional Unit 4.6: High side floating supply - The high side floating supply is necessary for driving the gate drive circuit, allowing 100 % duty cycle operation.

Functional Unit 4.7: Protection circuitry - If for example over current is detected on the output of the power amplifier, the switching devices need to be shut down and the controller notified of the fault condition. The protection circuitry will deactivate the PAs under the following conditions:

- Over temperature;
- Over current;
- Short circuiting (pulse for pulse).

Functional Unit 4.8: Filters - The filters on the supply is necessary for removing transients and surges on the input supply [22].

3.2 Subsection functional capability flow

The integrated controller needs to be able to perform certain functions in order to satisfy all the requirements that initiated this project. The following sections define the functions and couples performance parameters to them where applicable.

3.2.1 AMB functional flow

The functional flow in Figure 3.5 captures the basic top level functions associated with the suspension of an AMB. That is, the rotor position needs to be determined by some type of sensor, an algorithm generates the correct control signal for the power amplifiers and an output current is supplied to the electromagnets that applies a greater or smaller force to the rotor.

Functions are labelled F x.x as can be seen in the figures. Figure 3.6 represents a functional flow of how the user will typically use the integrated controller. The flow is basically a breakdown of Function block F2.0.

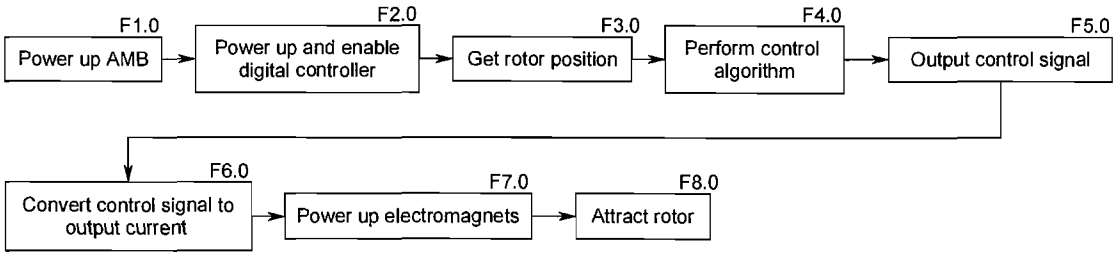


Figure 3.5: Functional flow of the AMB system

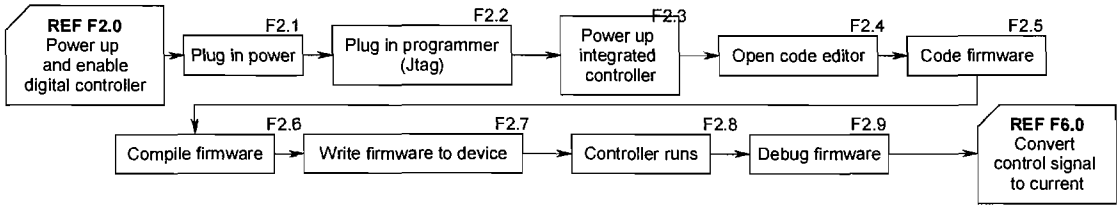


Figure 3.6: Using the integrated controller: functional flow

3.2.2 Functional capabilities of the controller

The breakdown of function F 2.8 can be seen in Figure 3.7 and represents the embedded controllers and surrounding electronics' functions.

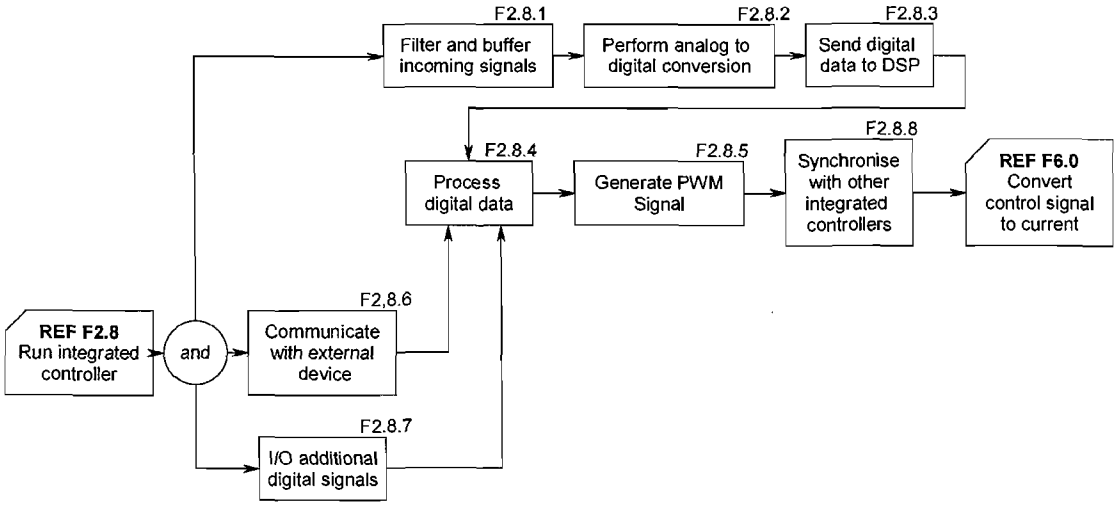


Figure 3.7: Functions of the integrated controller

Function F 2.8.1: Filter and buffer incoming signals - Functional unit 2.0, the analogue circuitry is responsible for performing this function.

Function F 2.8.2: Perform analogue to digital conversion - Analogue to digital converters (ADCs) will be implemented for signal digitization. The main embedded device contain integrated ADCs. The co-processor on the other hand does not have integrated ADCs and requires external devices. All signals that is used in the classic AMB operation will be routed to the main embedded device. Signals that are to be used in experimental self-sensing will be sampled by an external ADC and sent to the co-processor.

Table 3.2 summarizes the ADC requirements and Figure 3.8 illustrates a visualization of the analogue input signals and where they should go.

Function F 2.8.3: Send digital data to DSP - The external ADCs have to send the digitized signals to the FPGA through an interface link such as the Serial Peripheral Interface (SPI).

Function F 2.8.4: Process digital data - The main embedded device and the co-processor will run control algorithms for suspending the AMB. Minimum specification for MIPS is 150.

Function F 2.8.5: Generate PWM signal - The control algorithm determines the PWM signal that will be applied to the power amplifier's switching devices.

1. The PWM signals will range from 20 kHz to 50 kHz.

Table 3.2: ADCs allocation and requirements

Signal input type	**ADC minimum specifications**	**Interface with:**	**Amount of ADCs required**	**Available for**
Position signals	100 ksps, Single ended, 0 to 3.3 V	Main embedded device	1	External
Additional external signals	100 ksps, Single ended, 0 to 3.3 V	Main embedded device	3	External
Power amplifiers	100 ksps, Single ended, 0 to 3.3 V	Main embedded device	2	PA current sense
Additional sense signal	1 Msps, Differential, -10 to +10 V	Co-embedded device	4	PA additional sense
Remaining analogue inputs of main embedded device	2 Msps, Single ended, 0 to 3.3 V	Main embedded device	10	I/O expansion area

2. The duty cycle will be variable between 0-100 % with at least 1024 intervals over the variable range.

Function F 2.8.6: Communicate with external device - The integrated controller will have communication interfaces that will meet the following requirements:

1. An RS485 driver will be implemented capable of a maximum bit rate up to 20 Mpbs
2. An RS232 driver will be implemented.
3. The integrated controller shall also have an USB interface. The interface shall be USB 2.0 compliant. Maximum bit rate need only be 12 Mbps.

Function F 2.8.7: I/O additional digital signals - Additional signals refer to functional unit FU 10.0 in Figure 3.1.

Function F 2.8.8: Synchronize with other integrated controllers The synchronization signal is illustrated as Functional unit FU 13.0 in Figure 3.1. In order to meet the specification for the PWM signal of maximum 50 kHz and 1024 different duty cycle settings, the synchronization signal will be maximum $50e3 * 1024 = 51.2$ MHz. This signal may then be used to clock the PWM generator.

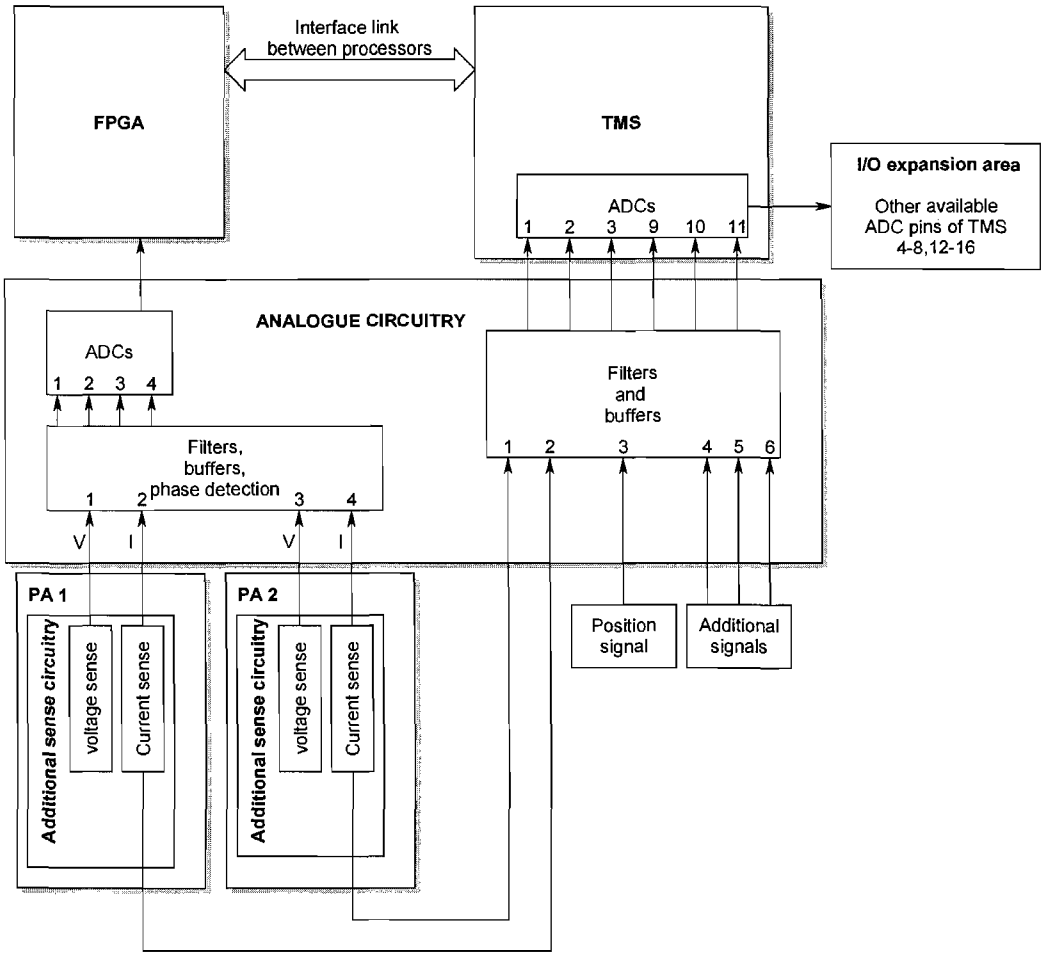


Figure 3.8: Analogue input signals

3.2.3 Functional capabilities of the power amplifiers

Breaking down the function F 6.0, convert control signal to output current, allows for the specification of the power amplifier functions as illustrated in Figure 3.9.

Function F 6.1: Isolate incoming PWM signals - The isolation device should have a relatively low propagation delay time as well as low rise and fall times. Maximum time parameters will not exceed 100 ns.

Function F 6.2: Drive 3-phase bridge - The driver for the switching devices will adhere to the following specifications:

1. Maximum high side floating supply voltage: 400 V (the driver must tolerate at least 400 V on its pin that connects to the output of the high side switching device);
2. Maximum propagation delay time: 200 ns;

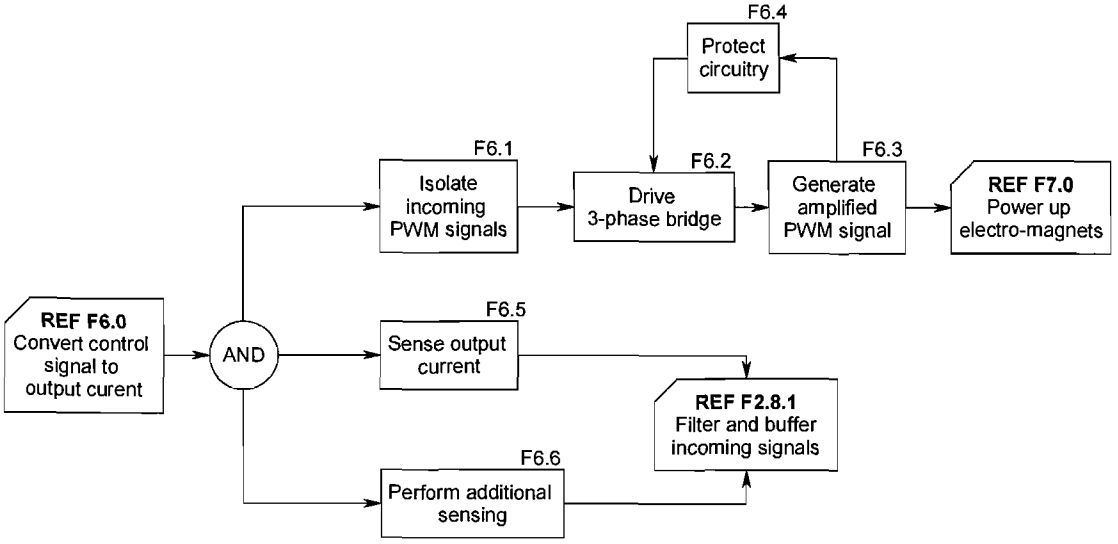


Figure 3.9: Functions of the power amplifier

3. Maximum rise and fall time of signals: 50 ns;
4. Voltage and current rating will depend on switching device used.

Function F 6.3: Generate amplified PWM signals - Nominal specifications for the switching devices that will be used in the power amplifiers are the following:

1. Bridge voltage variable between 50 to 310 V with a 10 % tolerance.
2. Output current: 7.5 A rms; 15 A peak
3. Maximum switching frequency 50 kHz.

Function F 6.4: Protection circuitry - The protection circuitry will shut down the power amplifiers or at least generate a warning signal for the embedded processor under the following conditions:

1. Over temperature. If the ambient temperature of the switching devices exceeds a certain value, the power amplifiers will be shut down. This value will be determined from the maximum temperature rating of the power devices. A typical value will be 75 °C. A linear sensor will be implemented for temperature monitoring. The accuracy of the temperature sensor will be no less than 2.5 °C.
2. The switching devices of the power amplifier will be switched off if the output current exceeds the specified peak of 15 A. The current limit mechanism will operate pulse for pulse, meaning that the current should be limited only a pulse at a time and not indefinitely when over current is detected
3. If an indefinite short is applied on the outputs of the power amplifiers, the switching device will be switched off.

Function F 6.5: Sense output current - A current sensor will be implemented with the following specifications:

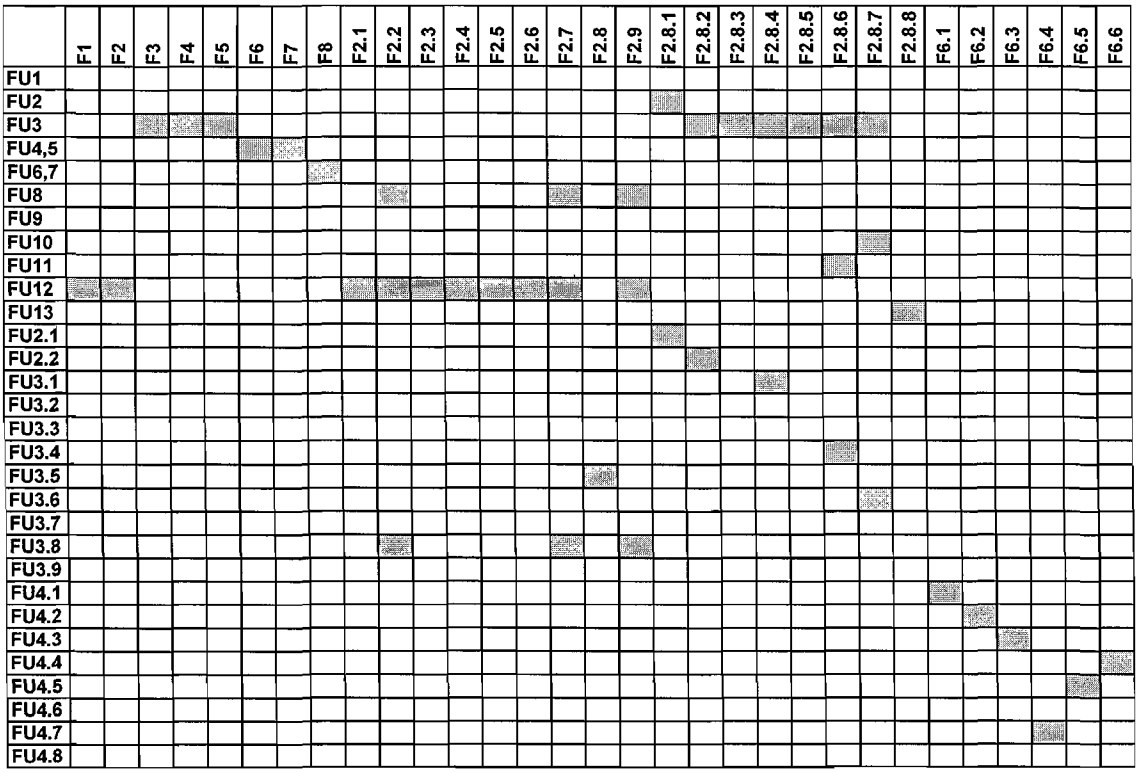
1. Maximum current: 30 A;
2. Minimum bandwidth: 100 kHz;
3. Minimum accuracy: 0.5 %.

Function F 6.6: Perform additional sensing - Additional sensing besides current sensing, is extracting the output voltage signal of the power amplifiers. This will be done with the use of divider resistors.

3.2.4 Allocations

All the functions can be linked to at least one functional architecture, that is each function has an architectural unit that performs, or is used for that function. Table 3.3 shows the relationships between the functions and the functional architectural units. By linking functions with architecture, traceability is kept between the phases of the system development process.

Table 3.3: Function link table



3.2.5 Resource allocation

Although most of the designs are collaborative approaches between the McTronX research group and an industry partner, the highest workload for specific elements in the development process was divided as shown in table 3.4.

Table 3.4: Work allocation table

	McTronX	Industry partner	Sub-contractor
Detail specification development	X		
Project management	X		
Analogue circuitry design	X		
Digital circuitry design		X	
Power electronics design		X	
Communication interfaces design	X		
PCB layout		X	
PCB manufacturing			X
System initial testing	X	X	
System evaluation	X		

3.3 Mechanical requirements

For a complex system that integrates power electronics, digital electronics and analogue electronics it is good practice to partition the PCB layout into a section for each type of electronics [8]. In this design it was seen fit to separate power, digital and analogue electronics into three separate PCBs and then piggy-back them on top of one another using appropriate connectors.

If the system in Figure 1.3 is considered, it can be seen that six integrated controllers are

required if the system is set up in the manner illustrated. Two controllers are required per radial bearing and one for the axial bearing. In a system with two radial bearings, one axial bearing and a main controller, six controllers are required. For this reason the integrated controller will be mountable in a subrack in order to keep the integrated controllers together in an organized array.

Using previous designs as reference for the space that the electronics will occupy on a PCB, the PCB sizes for this system was specified to be *Double Euro* sizes: 158.75 x 234.95 mm (6.25 x 9.25 in). Only the PCB with the analogue circuitry will be shorter for better partitioning. The analogue circuitry will be piggy-backed on a PCB containing electronics including digital circuitry and power supplies such as a flyback converter. The power supplies will for example be partitioned not to be directly under the analogue circuitry. The digital circuitry on the other hand, such as the embedded controllers, will be directly underneath the analogue circuitry, since they need to interface with one another with as short as possible PCB tracks.

A front view of a 6 U subrack with guide rails is illustrated in Figure 3.10. A subrack that is capable of mounting a Double Euro PCB is specified as a 6 U subrack. The figure is only representative of the subrack and in no means a scaled drawing. It serves only to illustrate the dimensions of the area where the PCBs will be mounted.

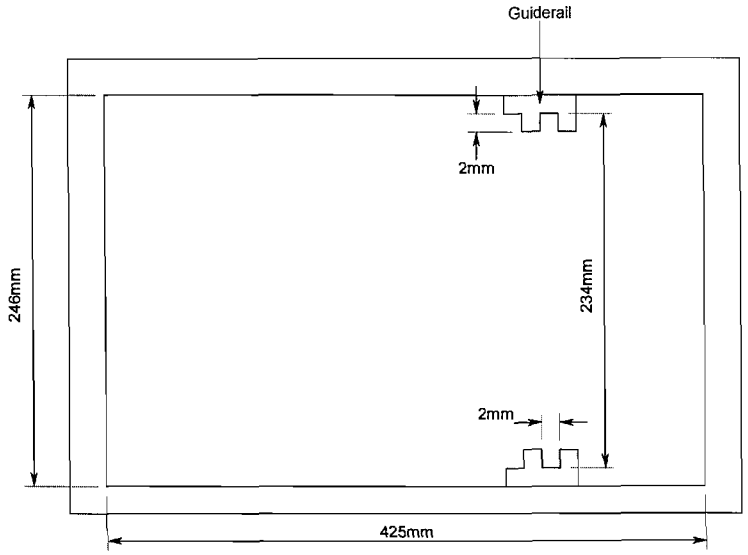


Figure 3.10: Typical 6U Subrack dimensions

A front view of the integrated controller is presented in Figure 3.11, as it would be seen from the front when placed in the subrack. The three PCBs are shown with certain dimensions specified. In order for the integrated controller to slide into the guide rails of the subrack, the substrate will be machined to have flanges that will fit into the guide rails.

The substrate in this case is an aluminium layer and a copper layer with a ceramic layer

between them. The circuits are etched into the copper layer (which can be only a single layer). This provides excellent heat dissipation of the high power devices soldered onto the printed circuit.

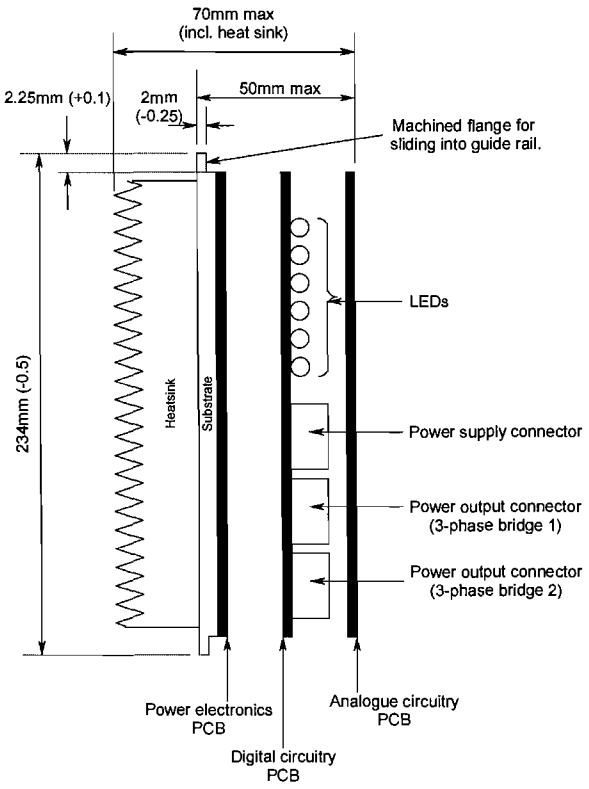


Figure 3.11: Front view of integrated controller

The total width of the PCB substrate will not exceed 234 mm, since that is the distance between the guide rails of the subrack. The printed circuit area's total height will be at least 4.5 mm less than the substrate's width to provide room for the 2 mm flanges of the guide rails.

Total width of a typical 6U subrack is 425 mm. If six integrated controllers are to fit into the subrack side by side, the total height of the integratd controller will not exceed 70 mm. This includes a heatsink that can be mounted to the substrate of the power PCB. 20 mm is enough room for a heatsink, leaving the three piggy backed PCBs' height to be no more than 50 mm.

At the front of the integrated controller (the front seen once slided into a subrack) will be LEDs and the power connectors. The power connectors include both input power to the system and the output connectors of the two 3-phase bridges on the integrated controller. At the back of the integrated controller will be the connectors for the sensitive signals such as the analogue inputs and programming interfaces. This configuration effectively separates the high power signals from the low power signals, reducing the chances of unwanted noise on sensitive input/ouput signals.

A face plate could be mounted on the front of the integrated controller to reveal only the protruding LEDs, power connectors and switches. Figure 3.12 shows a top view of the integrated controller and presents it with a face plate at the front.

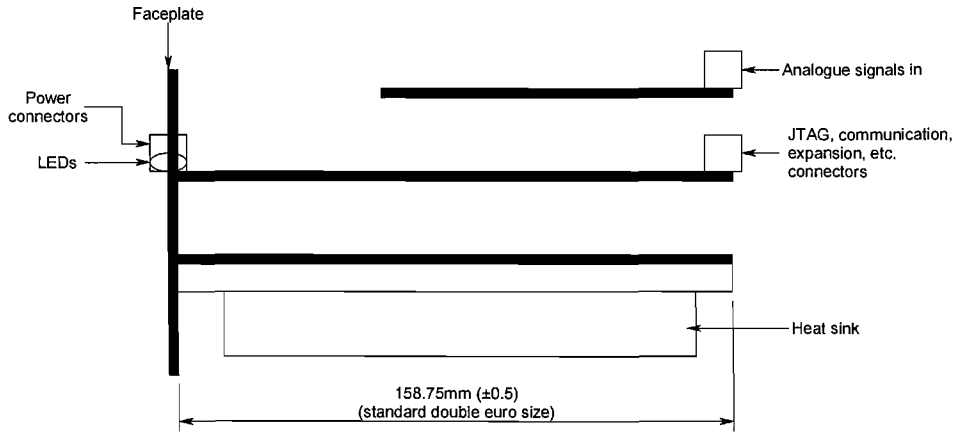


Figure 3.12: A top view of the integrated controller

Mounting a faceplate on the integrated controllers and placing them in a subrack will round off the appearance of the control system and bring the realization of an industry standard control rack closer. In order to attach a face plate, keep out areas are assigned on the power and digital PCBs where holes can be drilled and the plate attached with brackets. This is illustrated in Figure 3.13.

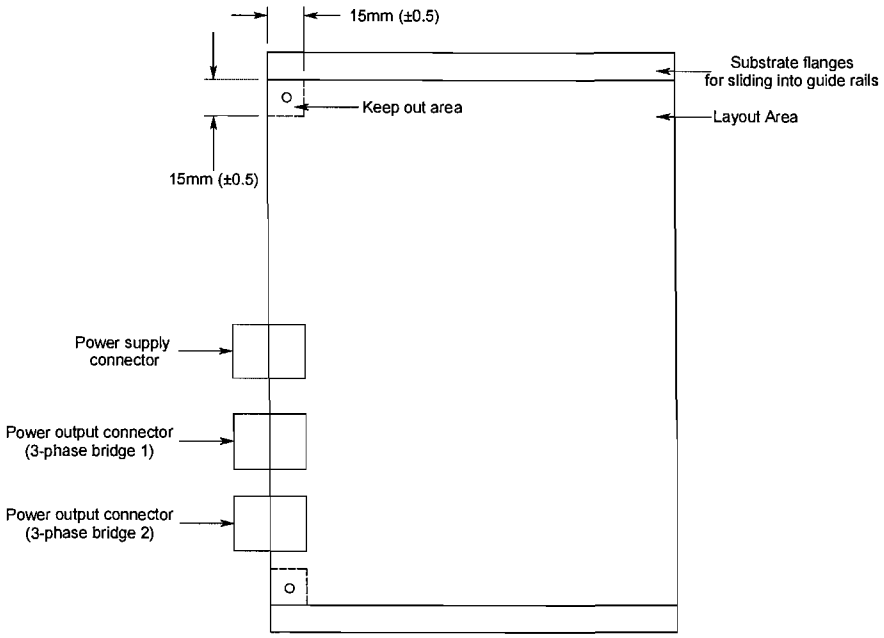


Figure 3.13: Side view of integrated controller showing keep out areas

3.4 Conclusion

This concludes the integrated controller's specification. In Chapter 4 to follow, design and evaluation results will be presented on embedded devices and RS485 communication architecture. This will motivate the embedded devices and communication architecture specifications.

Chapter 4

Sub-system design and evaluation

Chapter 4 evaluates certain algorithms and their execution time on specific embedded devices. Furthermore, a simple RS485 communication interface is implemented for evaluation purposes. The results in each case are used to motivate design choices.

4.1 Embedded devices

In the preliminary design phase of the system certain choices were made regarding the embedded devices to be implemented in this project. The following section will discuss some of the motivations for the device choices.

4.1.1 DSP

In order to implement control algorithms, a suitable embedded device was needed. A Texas Instruments DSP, the TMS320F2812, appealed as the first convenient choice because of the following:

- The McTronX research group and the industry partner have experience with this specific device;
- An AMB has already been suspended with this device in a previous Masters project;
- The development tools for this device have already been purchased and thus the development environment is familiar.

The TMS320F2812 boasts a wide variety of features that include DSP architecture and peripherals typically found on a controller. With digital signal processing capabilities and controller features the TMS320F2812 is a powerful device offering the best of both worlds. The device's features can be summarized as follows:

- High performance 32-bit CPU
  - 150 Million Instructions per second (MIPS) or one instruction every 6.67 ns.
  - 16x16 and 32x32 Multiply and Accumulate (MAC)
  - Harvard bus architecture
- On-chip memory
  - 128K 16-bit word Flash
  - 128K 16-bit word ROM
  - 18K 16-bit word Single-Access RAM
- External interface
  - Up to 1M external memory interface
- Motor control peripherals
  - 16 PWM outputs
- 16 Built in ADCs
  - 12-bit
  - Conversion rate: 80 ns/12.5 Msps
  - Two sample and hold units
- Serial port peripherals
  - Serial peripheral interface (SPI, synchronized serial port)
  - Two Serial Communication Interfaces (SPI), Standard UART
  - Enhanced controller area network (CAN)
  - Multichannel buffered serial port (McBSP)
- 56 General Purpose Input/Output (GP I/O) pins
- Three external interrupts
- Three 32-bit CPU timers

Since the integrated controller's main function is for the implementation and investigation of self-sensing, processing power is an important aspect to consider when choosing an embedded device and will be discussed in the following section (4.1.2).

4.1.2 Computational complexity

In digital signal processing applications one or more of the standard signal processing components (e.g. Filters, FFTs) will always be present. To determine the processing power required of the embedded controller, the computational intensity of these DSP functions will be investigated, specifically the functions that will be most likely used in the self-sensing algorithms.

To roughly predict the processing power required by an embedded device to execute an operation, the amount of CPU cycles need to be determined for that operation. A CPU cycle is the time it takes for the CPU to complete an instruction cycle (fetch, decode, execute).

Finite Impulse Response Filter (FIR) An N^{th} order FIR filter can be described by (4.1)

$$y(n) = \sum_{k=0}^{N} h(k) \times x(n-k) \tag{4.1}$$

where $h(k)$ are the impulse response coefficients. [9]. For each operation a multiplication and a summation are required. The MAC function of the DSP could be used for this operation which multiplies and accumulates the answer with one instruction. The MAC instruction still requires 2 CPU cycles though. A 100^{th} order filter would still require 200 cycles to execute as can be seen in Table 4.1.

Table 4.1: Cycles required for a 100^{th} order FIR filter

	Multiplications	**Additions**	
N^{th} order FIR	N	N	
Cycles using MAC	1	1	
Total cycles	N	N	2N

Fast Fourier Transform (FFT) When the FFT is applied in the time domain it is referred to as a decimation in time (DIT) FFT. This is because of the reduction in the number calculations when using a DIT algorithm as oppose to a normal discrete fourier transform (DFT) algorithm. The DIT FFT technique is also referred to as the butterfly FFT [9]. Table 4.2 shows the number of multiplications and additions for both DFT and FFT algorithms. Texas Instruments provides a FFT library that can be used to implement FFTs on a TMS320F2812. According to [23] the amount of cycles a 512 FFT will take is approximately 62 146.

4^{th} order nonlinear function 4.2 is a 4^{th} order nonlinear function for which the calculations statistics are shown in Table 4.3.

$$y = ax^4 + bx^3 + cx^2 + dx^1 + k \tag{4.2}$$

Table 4.2: Number of multiplications and additions for DFT and FFT

	DFT		FFT	
	Complex Multiplications	**Complex Additions**	**Complex Multiplications**	**Complex Additions**
256 FFT	65 536	65 280	1 024	2 048
512 FFT	262 144	261 632	2 304	4 608
1024 FFT	1 048 576	1 047 552	5 120	10 240

Table 4.3: Cycles required for a 4^{th} order nonlinear function

	Multiplications	**Additions**	
4^{th} order	7	4	
Cycles	1	1	
Total	7	5	12

Proportional plus Integral plus Derivative (PID) control loop The PID control loop might not be a DSP function but its implementation in the digital domain is important because of its numerous application areas. PID control is applied in AMB systems, so the relevance is justifiable.

The transfer function of a PID controller in the w-plane is given in (4.3)

$$D(w) = K_P + \frac{K_I}{w} + K_D w \tag{4.3}$$

where K_P is the proportional gain, K_I is the integral gain and K_D the derivative gain. The gain of the PID filter will increase as the frequency increases, and thus (4.3) is not a practical approach. To solve the problem a pole can be added to the differentiator component. The pole is chosen far outside the bandwidth of the system thus has little effect on the response of the system. The transfer function of the PID loop then becomes [24]:

$$D(w) = K_P + \frac{K_I}{w} + \frac{K_D w}{1 + (w/\omega_{wp})} \tag{4.4}$$

The pole is chosen to be at:

$$\omega_{wp} = -\frac{2}{T} = -\frac{\omega_s}{\pi} \tag{4.5}$$

where ω_s is the sampling frequency and T is the sampling interval. By transforming (4.4) into the z-plane, 4.6 is obtained [24].

$$D(z) = K_P + K_I \frac{T}{2}\left[\frac{z+1}{z-1}\right] + K_D\left[\frac{z-1}{Tz}\right] \tag{4.6}$$

The PID control can be implemented by calculating the proportional, integral and differential gains separately and summing them at the output. Alternatively (4.6) can be transposed into a second order function [24]:

$$D(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{1 + b_1 z^{-1} + b_2 z^{-2}} \tag{4.7}$$

Where:

$$\begin{aligned} a_0 &= K_P + \frac{K_I T}{2} + \frac{K_D}{T} \\ a_1 &= -K_P + \frac{K_I T}{2} - \frac{2K_D}{T} \\ a_2 &= \frac{K_D}{T} \\ b_1 &= -1 \\ b_2 &= 0 \end{aligned}$$

The PID control is then implemented as a second order filter as shown in Figure 4.1. (4.8) is the difference equation describing the implementation structure [24]. This implementation requires two memory values, five multiplications and four additions (Subtraction can be regarded as an addition with a negative number).

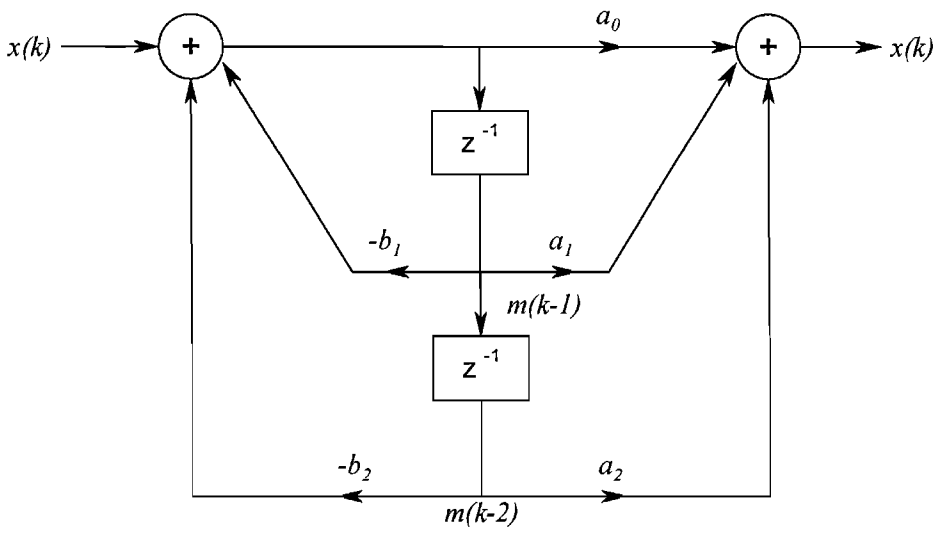


Figure 4.1: Second order filter structure

$$\begin{aligned} m(k) &= x(k) - b_1 m(k-1) - b_2 m(k-2) \\ y(k) &= a_0 m(k) + a_1 m(k-1) + a_2 m(k-2) \end{aligned} \tag{4.8}$$

A self-sensing algorithm could use multiple DSP functions. To be determined is the total amount of cycles a self-sensing algorithm would require. Table 4.4 summarises the amount of DSP functions that would be used in a self-sensing algorithm and their respective cycle times. These cycle times are only first order calculations and represents about 80% of the total processing power needed. The other 20% will include process management, communication, etc.

Table 4.4: Total cycles required for a self-sensing algorithm

	Cycles	**Amount**	**Total**
100^{th} order FIR	200	8	1600
512 FFT	62 146	2	124 292
4^{th} order function	12	1	12
Total	62 358		125 904

The control loop for McTronX's AMB model executes at 20 kHz or once every 50 µs. If the TMS320F2812 operates at 150 MIPS, one instruction cycle takes 6.67 ns. In a time span of 50 µs the DSP can execute approximately 7496 instruction cycles. Comparing this to the amount of cycles in Table 4.4 it can be seen that 7496 is only about 6% of the total cycles needed. The FFT algorithm is the most power hungry and represents almost 99% of the total processing power required. Clearly if an FFT is to be implemented in real time a co-processor is needed to share some of the DSP's processing load.

4.1.3 FPGA

The FPGA chosen for this application is a Xilinx® Spartan™-3E device. Xilinx offers a range of FPGAs but the Spartan-3E series is part of a low cost series designed for the high volume market. The Spartan-3E still offers a high number of features that will now be discussed.

System gates ranging from 100 K to 1600 K are available on the Spartan-3E. A middle tier FPGA with 500K system gates was chosen for this application. Table 4.5 summarises the attributes of the Spartan-3E with device code XC3S500E [25].

Multiplier Block [25] The integrated multipliers can accept two 18 bit values as input for multiplication.

Table 4.5: Attributes of Spartan-3E FPGA

Device	XC3S500E
System gates	500 K
Equivalent logic cells	10 476
Total CLBs	1 164
Total Slices[1]	4 656
Distributed RAM bits[2]	73 K
Block RAM blocks	20
Block RAM bits[2]	360 K
Dedicated Multipliers	20
Digital Clock Managers (DCMs)	4
Maximum User I/Os	232
Maximum Differential I/O pairs	92

[1] 4 slices in one Configurable Logic Block (CLB)

[2] One Kb is equivalent to 1024 bits

DCMs [25] The digital clock managers are capable of distributing, delaying, multiplying, dividing, and phase-shifting clock signals.

I/O capabilities [25] The FPGA offers a range of I/O standards in both single ended and differential interfaces. Supported single ended standards are:

- 3.3 V low-voltage transistor-transistor logic (LVTTL);
- Low-voltage CMOS (LVCMOS) at 3.3 V, 2.5 V, 1.8 V, 1.5 V, or 1.2 V;
- 3 V Peripheral component interconnect (PCI) at 33 MHz, and in some devices, 66 MHz;
- High speed transistor logic (HSTL) I and III at 1.8 V, commonly used in memory applications;
- Stub series terminated logic (SSTL) I at 1.8 V and 2.5 V, commonly used for memory applications.

The differential standards that the Spartan-3E FPGA supports are:

- Low voltage differential signalling (LVDS)
- Bus LVDS
- mini-LVDS
- Reduced swing differential signalling (RSDS)
- Differential HSTL (1.8 V, Types I and III)
- Differential SSTL (2.5 V and 1.8 V, Type I)
- 2.5 V Low-voltage positive emitter-coupled logic (LVPECL) inputs

As was seen, FFT calculations consumes a lot of resources on the DSP. Table 4.6 shows the amount of resources a 1024 point FFT would use if implemented on an FPGA.

Table 4.6: Resources required if FFT is implemented on an FPGA

FFT point size	Slices	Block RAM	Multipliers	Time
256	1400	7	9	4 µs
1024	1500	7	9	16 µs

Comparing Tables 4.6 and 4.5 it can be seen that the following percentage of the resources are consumed: 32% of the slices, 35% of the RAM and 45% of the multipliers. Since the FFT algorithm will consume the largest part of the resources compared to other codes that will be implemented on the FPGA, the Spartan-3E with 500 K logic gates would suffice for this application.

4.2 RS485 design

An RS485 interface was specified for the system because of its robustness and high data rate capabilities. To determine the maximum bit rate required for a worst case scenario, Figure 1.3 is considered. If the master controller is to communicate with each slave node, a typical procedure would be the following:

1. The master controller polls a node to inform it that data can be sent.
2. The slave node sends a 4x16 bit packet to the master controller.
3. The master controller sends data back to the slave controller.

This must happen five times within a control loop of 50 µs, once for every slave controller. The communication can be summarised as follows:

- 3 packets are sent between the master controller and a slave controller;
- There are 5 slave controllers;
- The control loop executes at 20 kHz;
- A data packets consists out of 4 words of data;
- One data word is 16 bits deep.

The maximum data rate in bits per second can then be calculated as:

$$3 \times 5 \times 20\,000 \times 4 \times 16 = 19.2 \text{ Mbps}$$

To verify that RS485 is a feasible option for a communication interface, a laboratory setup was used to investigate RS485 communication. A RS485 communication link was established between a development board containing a TMS320F2812 DSP and a dSpace system as can be seen in Figure 4.2. The Serial Communication Interface SCI of the DSP is used to interface with a RS485 driver circuit. The driver circuit converts the single ended SCI signals into RS485 differential signal levels. dSpace has its own RS485 interface to which the driver circuit is connected by means of a appropriate transmission line.

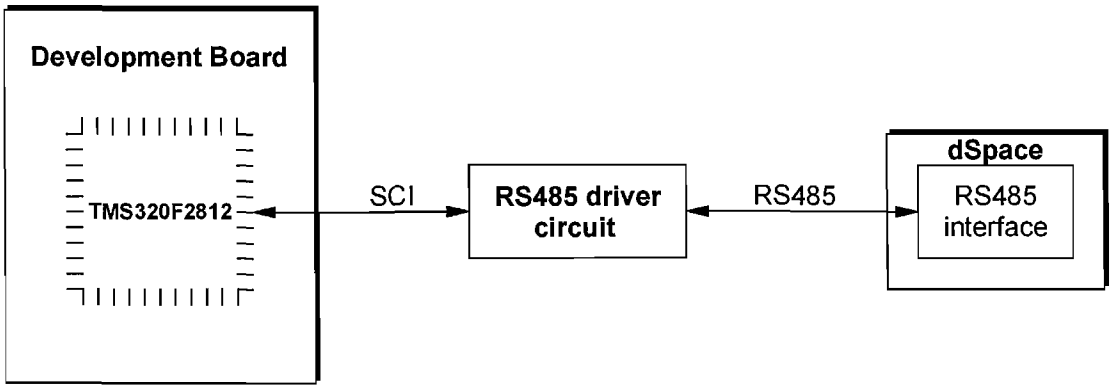


Figure 4.2: RS485 configuration for evaluation purposes

4.2.1 Characteristic impedance of transmission line

A CAT5e 20 m network cable was chosen for the transmission line. The characteristic impedance of the line is specified as 100 Ω at 110 MHz. For the purpose at hand the transmission line will be operating at a much lower frequency (approx. 500 kHz). In order to verify the characteristic impedance, an RLC analyser was used to measure the the resistance, capacitance and inductance of the transmission line at 50 Hz.

The total measured wire length was increased to approximately 160 m by connecting all four wire pairs of the CAT5e cable in series. Figure 4.3 illustrates the connections between the pairs of wires in the CAT5e cable. The orange pair's ends were used for connecting to the RLC analyser. The green pair's ends were left open for capacitance (C) measurement and short circuited for resistance (R) and inductance (L) measurements.

The RLC measurement values for the CAT5e cable was found to be the following:

R : 15.0142 Ω
C : 4 nF
L : 0.045 mH

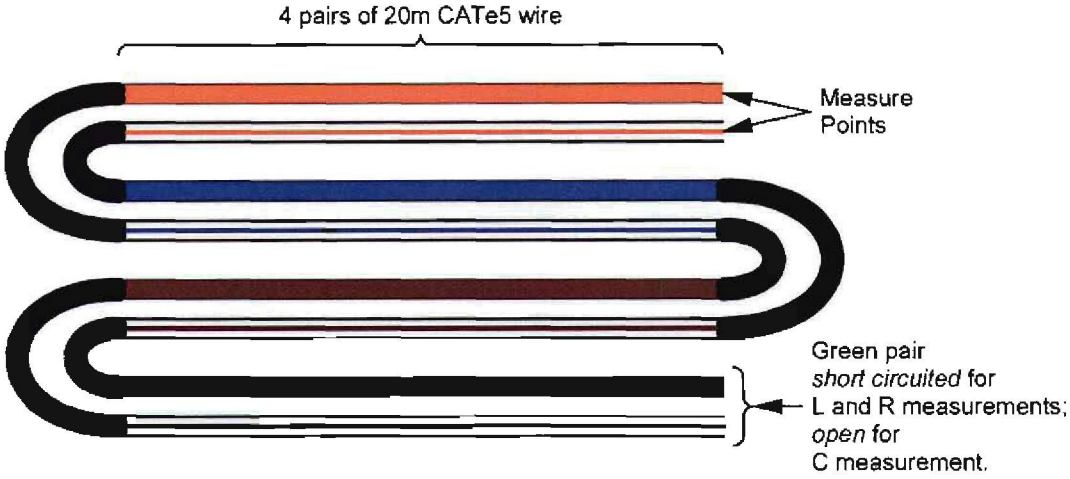


Figure 4.3: Series connections between wires in CAT5e cable for RLC measurements

According to [26] the Characteristic real impedance of a lossless line can be determined from (4.9).

$$Z_0 = \sqrt{\frac{L}{C}} \tag{4.9}$$

The characteristic impedance of the CAT5e cable is then calculated to be 106 Ω. It can be concluded that even at a significantly reduced frequency the CAT5e cable's characteristic impedance still remains well in the vicinity of 100 Ω.

4.2.2 Termination resistors

Termination is necessary to match the characteristic impedance of the transmission line to the impedance of the node. If the impedances are not matched the load will not absorb the transmission signal completely and some of the signal will be reflected back on the line.

To determine if termination is necessary, a good rule of thumb is to check if the propagation delay of the transmission line is more or less than the time interval of one bit [4]. The propagation delay of the signal refer to the time it will take for the signal to propagate 1 m of cable length. No termination will be necessary when the propagation time of a signal is a lot less than one bit length of the signal.

For this application the maximum baud is going to be 937500 bps, which has a bit length of 1.067 µ. The propagation delay of CAT5e cable is 548 ns. Multiply the propagation delay with a 20 m cable length and the total propagation delay is calculated as 10.96 µs for a 20m cable. Assume the signal will reflect and damp out in 3 round trips (one round trip is equivalent to 40 m cable). It will then take 6×10.96 µs $= 65.76$ µs for the reflections to damp out. The reflections take much longer to damp out than the width of a bit (reflection: 65.76 µs > bit width: 1.067 µs). It is thus necessary to put termination resistors on the line.

In section 4.2.1 it was seen that the characteristic impedance of the transmission line is in the vicinity of 100 Ω. In order to properly mach the line to the load, parallel type termination was chosen for the application with 100 Ω termination resistors. The 100 Ω termination resistors can be seen in Figure 4.5.

4.2.3 Bias resistors

When an RS485 network is in tristate mode (idle), all transceivers are in receive mode. The output of the receivers is then undefined. In order to force the data lines to a known state, biasing must be used. Biasing is nothing other than applying a pull-up resistor to the B line and a pull down resistor to the A line. Figure 4.4 illustrates the biased data lines.

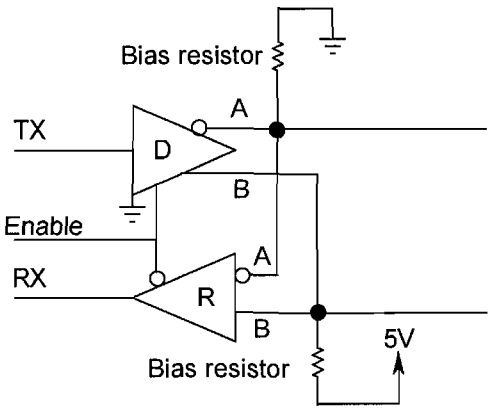


Figure 4.4: Biased data lines

If we take a node impedance to be 12 kΩ, and assume six nodes on the bus, the effective load impedance of 12 parallel nodes reduces to 2 kΩ.

The termination resistance was chosen to be 100 Ω. Two termination resistances in parallel gives a resistance of 50 Ω. The total impedance of the bus is thus the 50 Ω in parallel with the 2 kΩ which gives 48.78 Ω.

The termination resistors are thus dominant in the bus circuit because only two nodes are used

in this calculation. If the amount of nodes increases their impedances will play a larger role. For the remainder of the calculations 50 Ω will be used as the bus impedance.

A differential voltage of at least 200 mV is required to activate the receiver of the RS485 device. The current required to maintain 200 mV over the bus impedance is thus:

$$\frac{200e-3}{50} = 4\,\text{mA}$$

If the biasing is done from a 5 V supply, the resistance required to obtain 4 mA is:

$$\frac{5}{4e-3} = 1250\,\Omega$$

The total resistance of the network should thus be no more than 1250 Ω. To determine what the bias resistors should be, the following is done: The termination resistance is subtracted from the total network resistance which gives 1200 Ω. A resistor with a maximum resistance of $1200/2 = 600\,\Omega$ should thus be used for pull-up as well as pull-down. Figure 4.5 illustrates the designed RS485 network with termination and bias resistors.

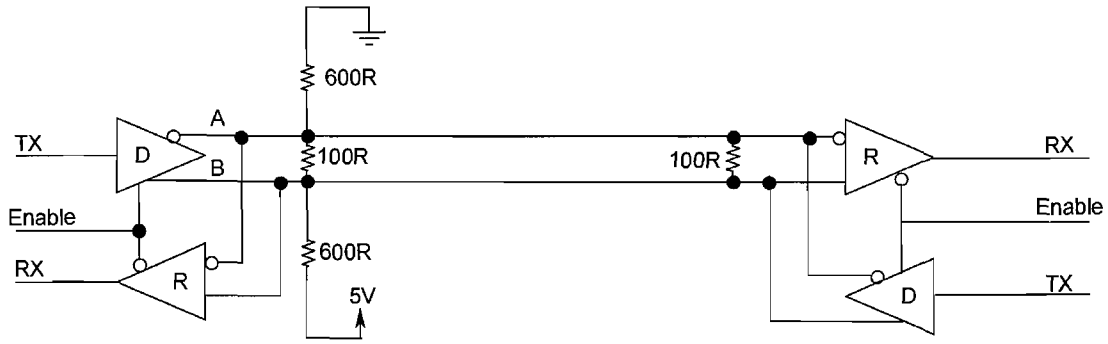


Figure 4.5: RS485 network with bias and terminating resistors

4.2.4 Implementation

The two devices need to communicate with each other is the dSpace PCI controller card and a TMS320F2812 DSP. The DSP is a 3 V device and dSpace operates at 5 V. In order to make the devices compatible, an optic isolation barrier was added to the RS485 interface circuit. The isolation separates the 5 V ground from the 3 V ground. Optic isolation also protects against transient currents that can cause voltages on the transmission line exceeding the RS485 interfaces' maximum ratings [4]. Figure 4.6 shows the interface circuit between the DSP and dSpace. The circuit lines on the 3 V side are connected to the SCI peripheral port of the DSP.

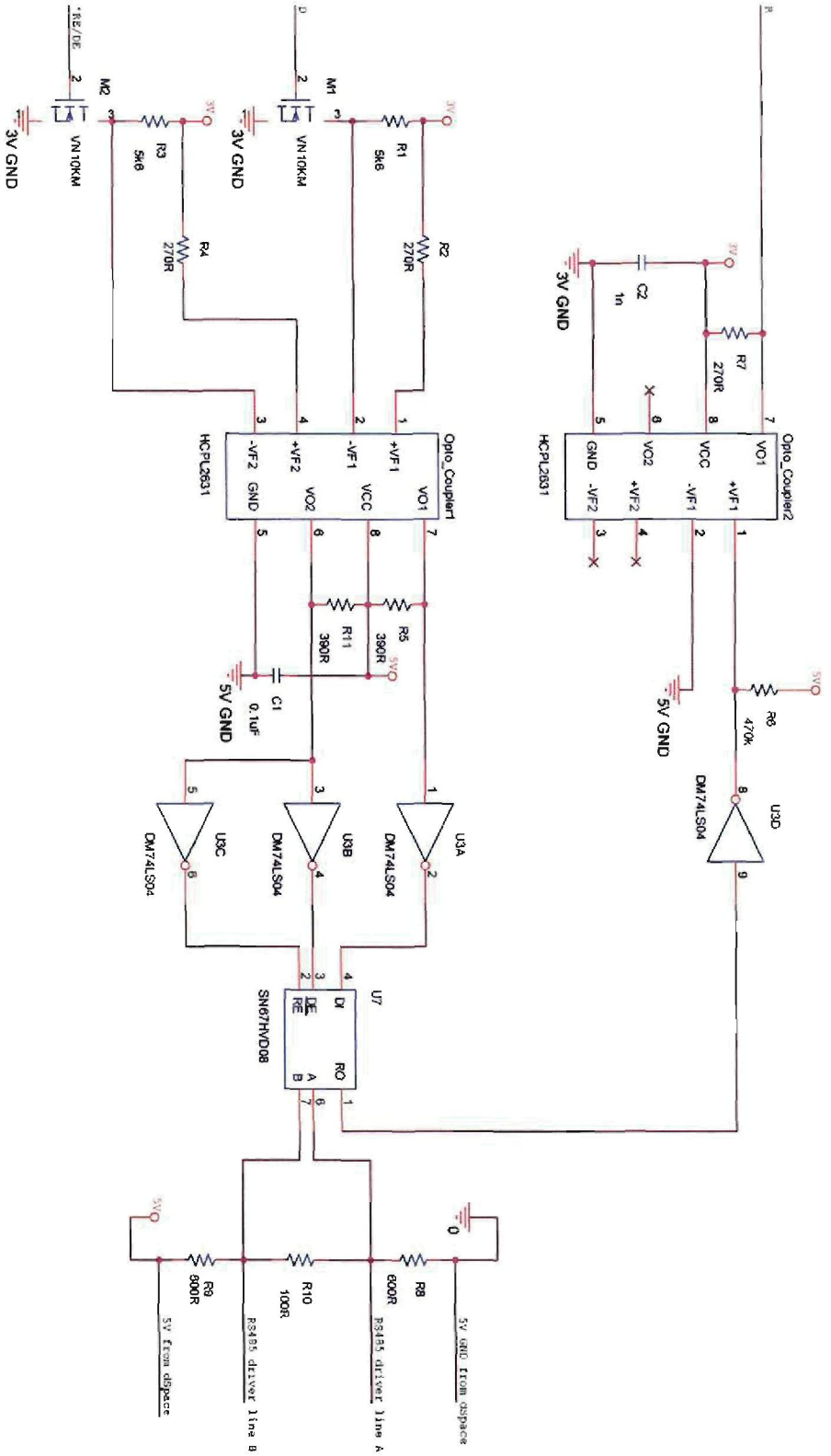


Figure 4.6: RS485 interface circuitry

The nominal output current of the DSP device is recommended to be 4mA. The opto-isolators require 10mA to operate properly. To alleviate the problem VN10KM MOSFETS was used as buffers between the DSP and the opto-isolators.

4.2.5 Evaluation

The evaluation of the RS485 communication was done at two different baud rates (292 969 bps and 937 500 bps) and with two different cable lengths (approximately 1 m and 20 m).

The baud rate values are non standard because both dSpace and the DSP allows for the setup of non standard baud rates. The baud rate values also allow for easy configuration of the DSP registers. Only one value in one register needs to be changed to switch between the two baud rates.

dSpace allows for only a maximum baud rate of 1 Mbps. The DSP was configured to 937500 bps. This is the closest baud rate that the DSP could be configured to without exceeding the maximum of 1Mbps.

Data loss

To test the data lost when the RS485 network is operating, the following procedure was followed:

1. An amount of data is generated by dSpace and sent over the RS485 network to the DSP. The data generated constitues unsigned integer values ranging from 0 to 255 since the buffer of the dSpace serial port is only 8 bits wide. The generated data is logged to a file.
2. The data is received by the DSP and then sent back over the RS485 network to dSpace.
3. dSpace receives this data and logs it to a file.
4. The data generated and the data received back from the DSP by dSpace is compared to check for any data errors.

This procedure is repeated ten times for both cable lengths and both baud rates. Table 4.7 summarizes the results.

Waveforms

Transmission signals were measured at the opposite end of the transmission line from where they were generated by the interface circuitry. Measurements were carried out and the data

plotted for all four combinations of the two baud rates and the two cable lengths.

Table 4.7: Summery of data loss results

Data rate	Cable length	Total amount of data points sent and received	Amount of data errors
292969 bps	1 m	250 000	0
292969 bps	20 m	250 000	0
937500 bps	1 m	400 000	0
937500 bps	20 m	400 000	2

Figure 4.7 illustrates the measurements for rise time (t_r) and unit interval length (t_{ui}) on the waveform obtained when the baud rate is 937500 bps and the cable length 1 m. These two time intervals are useful in determining if the waveforms are acceptable or not [6]. Table 4.8 gives a summery of the times obtained from the waveforms.

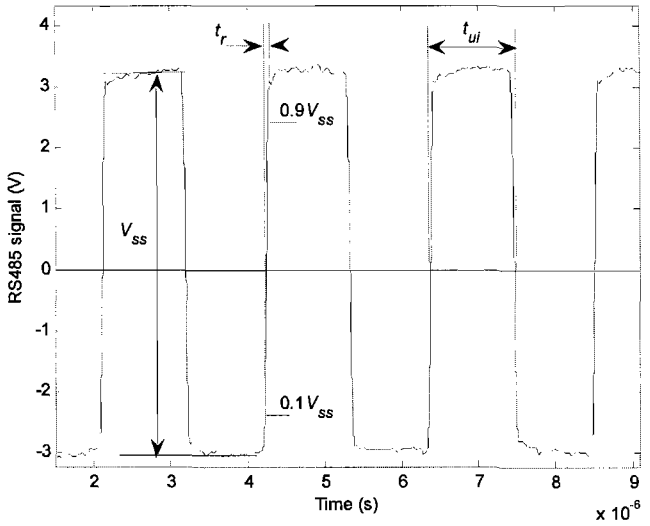


Figure 4.7: Baud: 937500 bps, 1 m cable

A good rule of thumb is that the rise time should be no more than 30% of the unit interval. As can be seen in table 4.8 all the rise times are well below 10% of the unit interval except the wave forms obtain with a data rate of 937500 bps and the 2 m cable. The waveform's rise time is approximately 20% which is still acceptable, and the receiver will still be able to extract legitimate data from the signal.

Table 4.8: Rise times and unit interval lengths of waveforms

Data rate	Cable length	Rise time (t_r)	Unit interval (t_{ui})	$t_r = \%t_{ui}$
292969 bps	1 m	51 ns	3.43 µs	1.5%
292969 bps	20 m	240 ns	3.44 µs	6.9%
937500 bps	1 m	52 ns	1.086 µs	4.7%
937500 bps	20 m	226 ns	1.152 µs	19.6%

Eye diagrams

The eye patterns are used to visually see the effect of noise, signal distortion and signal attenuation [6]. Figures 4.8 to 4.11 show the eye diagrams of the signal measured at again 937500 bps and 292969 bps with the two cable lengths. The eye diagram measurements were made at the same point as the waveforms.

Jitter is the measurement to determine the amount of distortion and noise that is present on the line. Jitter is the percentage that the waveform differs from the ideal state. Another way of looking at it is the thickness of the curves of the eye diagram [6].

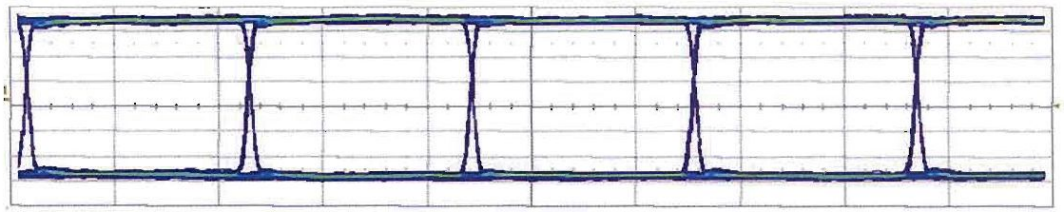


Figure 4.8: Baud: 937500 bps, 1 m cable

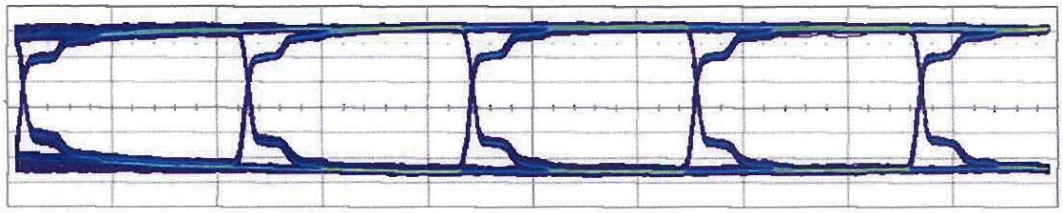


Figure 4.9: Baud: 937500 bps, 20 m cable

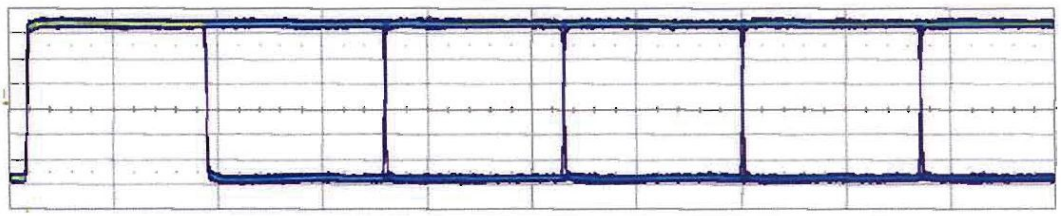


Figure 4.10: Baud: 292969 bps, 1 m cable

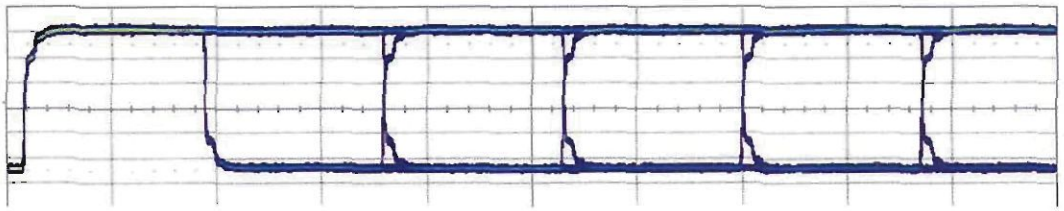


Figure 4.11: Baud: 292969 bps, 20 m cable

The most jitter can be seen in the eye diagram obtained from the signal with a baud rate of 937500 bps and a cable length of 20 m. The jitter on all the waveforms are within 5% which is an acceptable level [6].

4.3 Conclusions

4.3.1 RS485

RS485 offers robust communications even in noisy environments. RS485 proves to be very reliable if networks are designed correctly. As was seen the most important considerations include bit rate, transmission line length and the amount of nodes that will be present on the bus network.

In the evaluation of a very simple network involving only two nodes the differences between signals at different cable lengths and different baud rates are apparent. The longer cable introduces more signal distortion because of cable characteristics and possible outside interferences. RS485 drivers still produce waveforms acceptable for the receiver to read valid data.

This kind of reliability is almost impossible with normal single ended drivers such as RS232 which has only a single data line referenced to ground. RS485 allows for much higher bit rates and longer cable lengths and is a widely used industry standard.

4.3.2 Computational complexity

From the theoretical analysis of algorithms executing on both the DSP and FPGA, it can be seen that a lot of processing power and resources are required for the self-sensing algorithm. Especially the FFT, which has to be implemented on an FPGA, otherwise the time constraints will not be met. The actual execution times and resources required by the algorithms will be measured and presented in Chapter 5 to follow.

Chapter 5

Integrated controller hardware and evaluation

Chapter 5 shows the developed hardware sub-components (analogue-, controller- and power amplifier-PCBs) and a fully assembled integrated controller. The hardware's individual sub-components (ADCs, embedded devices, power amplifiers, etc.) are then evaluated to finally be integrated and be evaluated as a complete integrated controller system.

5.1 Integrated controller hardware

In this section the integrated controller's respective sub-systems will be shown and briefly discussed. Some of the functional components of the systems will be marked and referenced back to functional units (FU) specified in Chapter 3.

5.1.1 Analogue PCB

The analogue PCB contains the circuitry for conditioning of all analogue signals that need to be digitized and used in algorithms executing on the DSP and the FPGA. Table 3.1 in Section 3.1.1 shows the multiple analogue input signals. Of these signals only the position signal is imported via a DB9 connector shown in Figure 5.1. All other analogue signals (sensed current and voltage) enter the analogue PCB via inter-board connectors.

According to Table 3.2 in Section 3.2 four external ADCs should be interfaced to the co-embedded device which is the FPGA. These external ADCs are situated on the analogue PCB as seen in Figure 5.1. These ADCs are interfaced via a serial peripheral interface (SPI) that

requires high frequency clock signals. To minimize noise contamination of the analogue signals on the PCB, the interface connectors of the ADCs are situated directly underneath them. This minimizes track length to the FPGA.

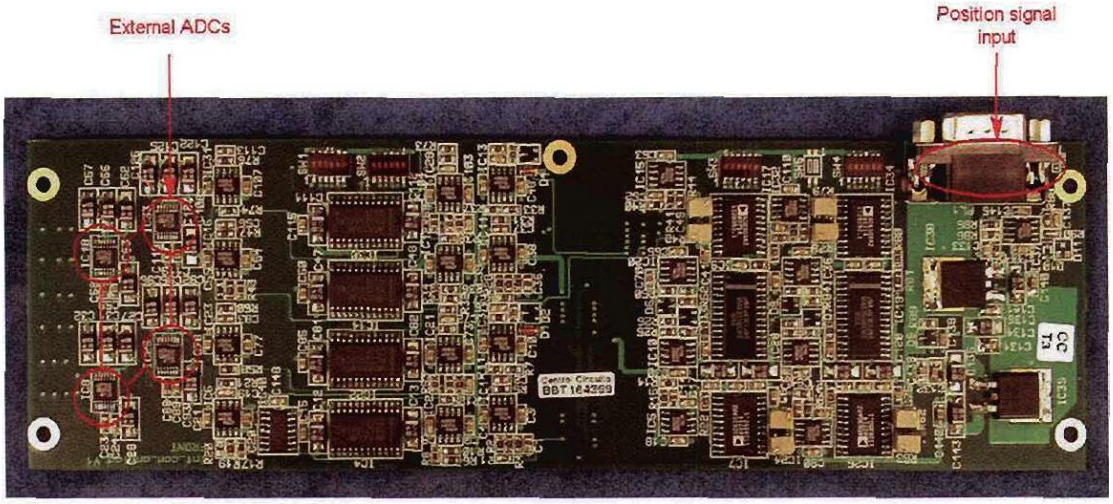


Figure 5.1: Analogue PCB

5.1.2 Controller PCB

The controller PCB contains most of the major components of the system. This includes the embedded devices (DSP and FPGA), input power connectors, output power connectors, power supplies, drivers for power amplifiers, communication interfaces, etc. In Figure 5.2 most of the major components are marked and referenced back to FUs specified in Chapter 3.

Marked with blue arrows, the inter-board connectors are shown in Figure 5.2 for connecting the analogue PCB to the controller PCB. As mentioned these connectors carry power and signals to and from the analogue PCB.

A ten layer PCB was necessary for the routing of the tracks because of the many components located on the controller PCB. Due to the board's complexity an overseas manufacturer was used. Overseas PCB manufacturers tend to produce higher quality PCBs, especially in the case of such complex PCBs.

5.1.3 Power amplifier PCB

The power amplifier PCB has only one layer on an aluminium substrate. The substrate based PCB is basically a 3.2 mm thick aluminium plane with a layer of copper on top. Between the aluminium and the copper is a layer of ceramic to isolate the copper from the aluminium.

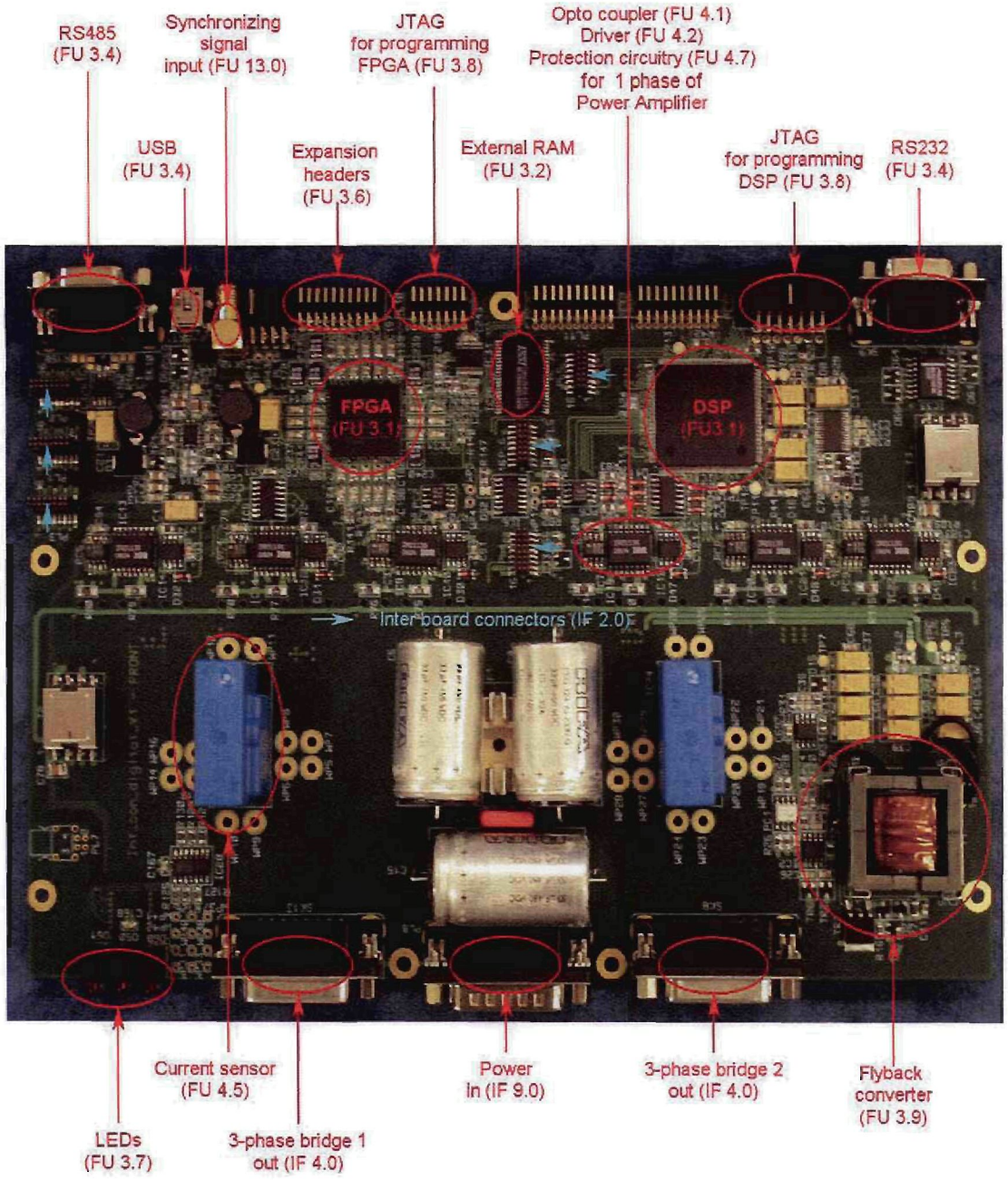


Figure 5.2: Controller PCB

Illustrated in Figure 5.3 is the power PCB with a total of twelve IGBTs and twelve free-wheeling diodes for the two 3-phase bridges.

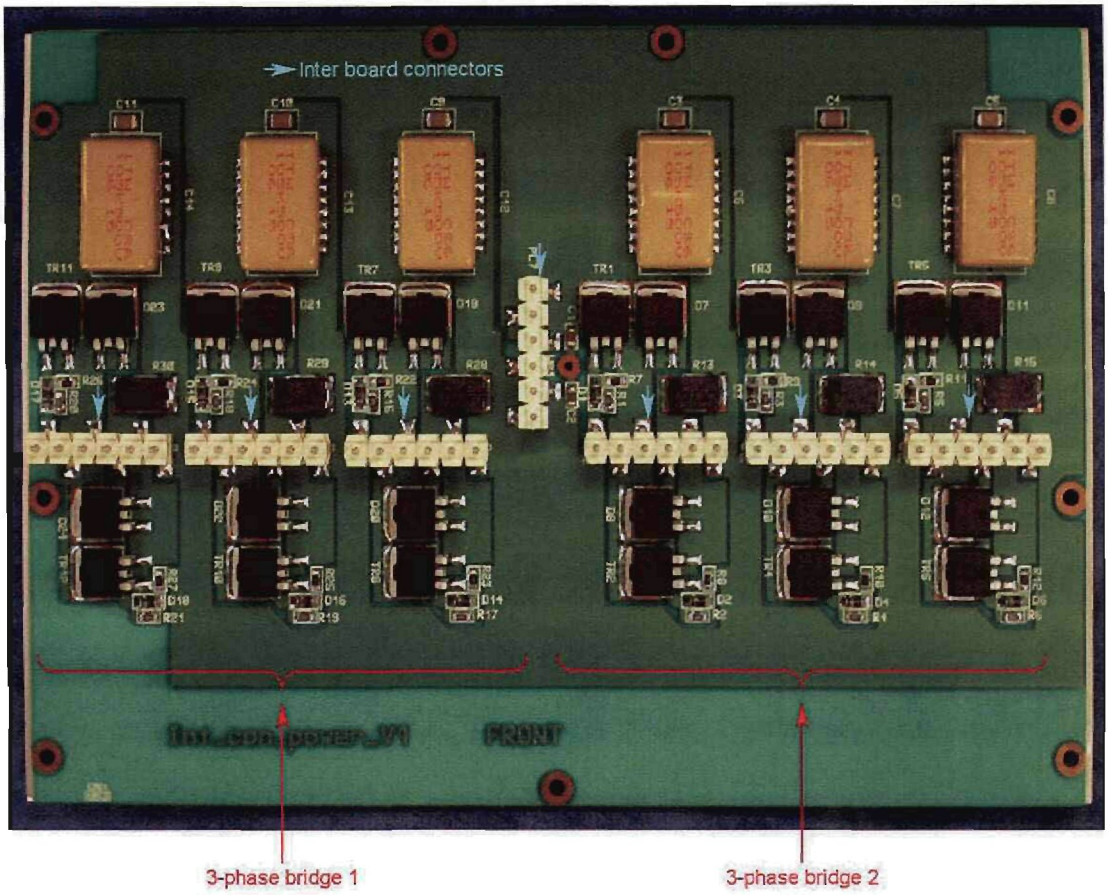


Figure 5.3: Power PCB

5.1.4 Integrated system

Figure 5.4 shows the analogue, controller and power PCBs assembled to form the integrated controller. Multiples of these integrated controllers can now be slid into a sub-rack to function as stand-alone systems or be controlled by a master controller.

The integrated controller is a generic system but was designed with self-sensing research in mind. The analogue PCB especially, is designed for conditioning signals so they can be used for self- sensing techniques. Since the integrated controller has a sub-system based architecture, the analogue PCB can easily be replaced by another PCB containing electronics for different signal conditioning applications.

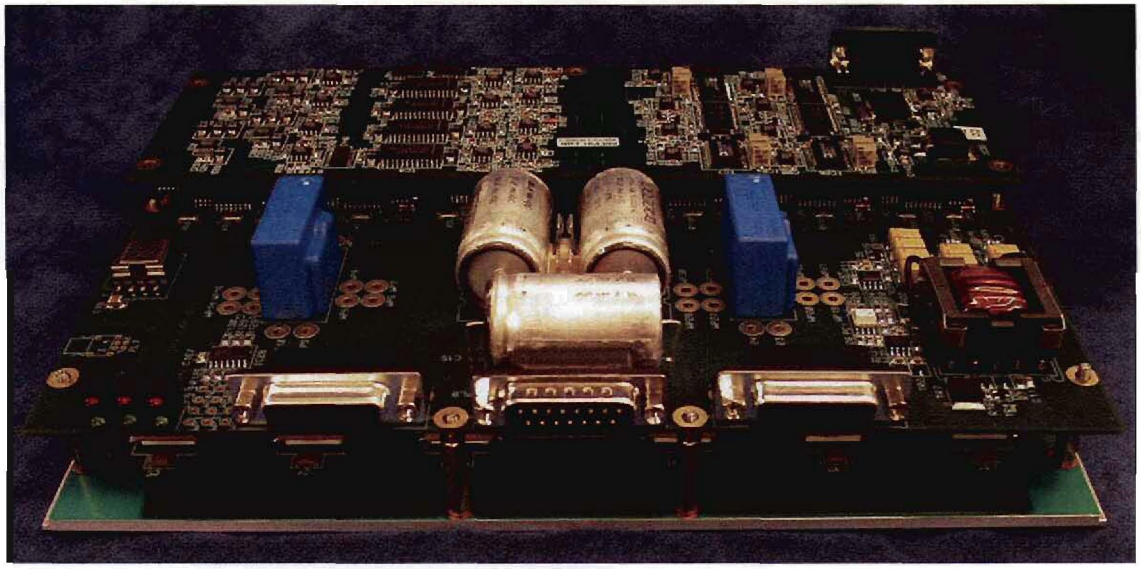


Figure 5.4: Integrated controller system

5.2 Evaluation

Now that the system hardware has been presented the evaluation proses for the integrated controller can be discussed. The process firstly involves the evaluation of the integrated controller's individual components and finally a configuration that will evaluate the system's functionality as an integrated system.

5.2.1 Evaluation process

This section only provides an overview of the evaluation process of the integrated controller. More detail and measured results on some sub-systems will be presented in sections to follow.

Check flyback outputs Once the integrated controller has been visually inspected for any apparent assembly faults, power can be applied to the flyback converter on the controller PCB. The outputs of the flyback converter are then measured for correct output voltages and polarities. The power pins of major components on the board such as the DSP and FPGA are checked for correct applied voltages.

The following evaluation procedures are only applicable to the controller PCB. The analogue and power amplifier PCBs are not attached to the controller PCB.

Program DSP Once satisfied that correct power is applied to the devices on the controller, a simple firmware program is loaded onto the DSP via the emulator to confirm that it can be correctly programmed. The first firmware loaded onto the DSP will configure the PWM registers of the DSP to generate a 20 kHz PWM with 50 % duty cycle and flash the LEDs

attached to the DSP at a frequency of 1 Hz. This piece of firmware will serve as a template for more complex algorithms to be added for further evaluation and configurations of the controller.

Check PWM outputs As mentioned, the DSP is responsible for generating PWM signals for the drivers of the IGBTs situated on the power amplifier board. An oscilloscope is used to check if the PWM signals are present in the following locations:

- Inputs of the opto-couplers;
- Outputs of the opto-couplers;
- Inputs of the IGBT drivers;
- Outputs of the IGBT drivers;

Configure FPGA A simple firmware program is used to configure the FPGA. The program toggles pins of the FPGA that are available on the expansion area of the controller, at a rate of 1 Hz. Using an oscilloscope, the pins are probed to confirm that the pins are toggling. As in the case of the DSP this simple piece of firmware will serve as a template for further algorithm implementation.

Establish communication between DSP and FPGA For this evaluation process some firmware needs to be added to the existing firmware templates.

A dual port RAM (DPR) block is implemented on the FPGA. DPR is as the name suggests, RAM that can be accessed from two different ports. One of the ports is used by the FPGA to write and retrieve data from the RAM, and the other port is used by the DSP to write and retrieve data. This is illustrated in Figure 5.5.

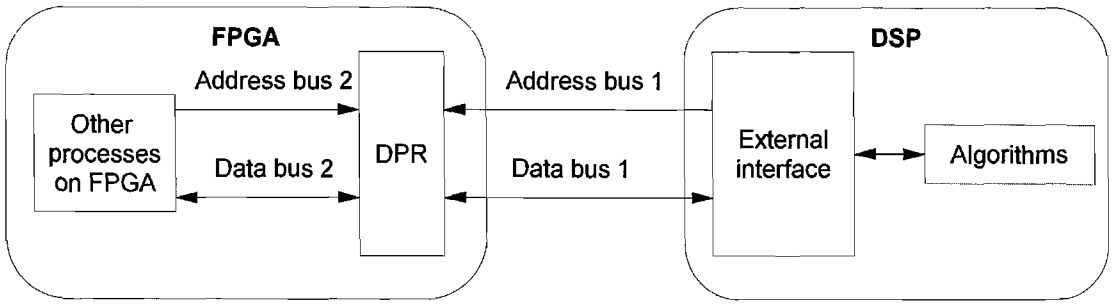


Figure 5.5: FPGA and DSP interface via dual port RAM

The FPGA places a constant value in a specific location in the DPR. The DSP reads this value from the DPR and places it in a variable. With the use of an emulator and debugging functions of the integrated development environment (IDE) Code Composer Studio™ (CCS) this value can be monitored in real time. If the variable's value coincides with the value being placed in the DPR by FPGA, the initial evaluation of the co-processor interface is successful.

Attach power amplifiers For the following evaluation procedures the controller is piggy-backed on the power amplifiers.

Perform initial tests on power amplifiers Power and a load is applied to the power amplifiers. By manually controlling the PWM duty cycle and voltage applied to the bridges of the power amplifiers, the following evaluations are performed:

- The voltage and duty cycle applied to the power amplifiers are increased slightly. With the use of differential voltage probes and a current clamp, the voltage across and current through the load are observed on an oscilloscope for any abnormalities.
- The power amplifier's over current protection is tested by increasing the voltage and duty cycle until the current through the load exceeds the specified peak current of 15 A.
- If the over current protection successfully limits the current in a pulse for pulse fashion, a short circuit test is performed. This is done by simply short circuiting the outputs of the power amplifier and verifying that the over current protection once again shuts down the IGBT drivers in a pulse for pulse fashion.
- Shorting the power amplifier causes pulse for pulse current spikes on the output of the power amplifier. The magnitude of these spikes are proportional to the voltage supplied to the power amplifier. To gather evaluation data the power amplifier is shorted at different supply voltage levels whilst measuring the magnitude the current spikes. The maximum current at maximum specified supply voltage can now be extrapolated from the collected data to determine if the current spikes would exceed the maximum peak current specifications of the IGBTs and free-wheeling diodes.

Attach analogue PCB The analogue PCB is piggy backed on the controller for the next evaluation procedures. This completes the integrated controller.

Evaluate analogue PCB Power on the analogue PCB is obtained from the flyback on the controller PCB. The voltages from the flyback are then regulated to the desired voltages on the analogue PCB. Using a multi-meter and oscilloscope these voltages are measured to confirm correct voltage levels to the components. The following measurements are then done on the analogue PCB:

- When power is applied to the power amplifiers and current is flowing through the load, the LEM sensors should produce a voltage on the inputs of the analogue circuitry proportional to the current through the load. This voltage level is observed with the use of an oscilloscope. The signal undergoes scaling before being placed on the inputs of an external ADC (See Figure 3.8 Chapter 3). The input signal is measured at the input of the ADC to check for correct voltage levels.

- A signal is placed on the position input of the analogue circuitry and measured before and after the conditioning hardware.

Current signal digital processing The following evaluation process involved further firmware development and implementation. The external ADCs require a serial peripheral interface (SPI). A piece of firmware is thus required on the FPGA that communicates via SPI to the ADCs in order to configure them and obtain the digitized signal data. The data is then filtered and placed in the DPR where the DSP can read it. Once again the value obtained by the DSP is observed using the emulator and compared to the actual current. The configuration is shown in Figure 5.6.

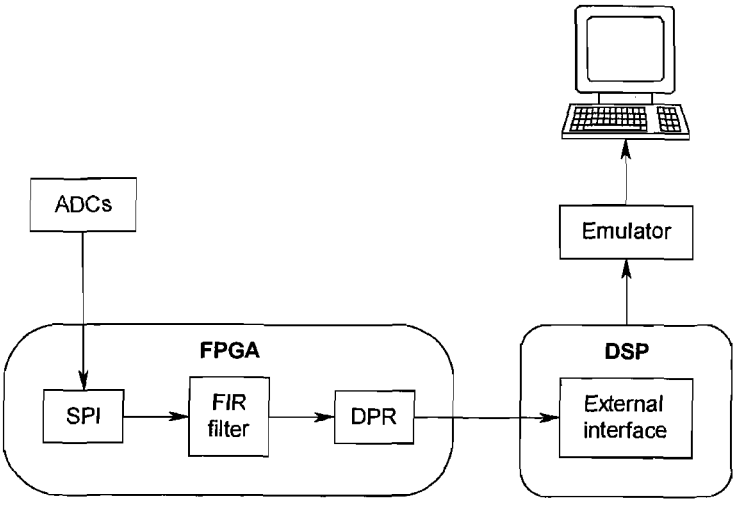


Figure 5.6: ADC interface evaluation

Design control algorithm At this stage, all the major components necessary to perform closed loop control on the current of the power amplifiers have been tested. A proportional an integral (PI) control algorithm is now designed and implemented on the DSP. The closed control loop can be seen in Figure 5.7. First the current reference is manually varied to confirm the control loop is operating properly. A sine wave reference is then applied to confirm the small signal and power bandwidth of the power amplifier.

5.2.2 Flyback converter outputs

Before any measurements can be performed on the integrated controller, power to the system has to be checked. The flyback converter is a switch-mode power supply that converts the input power to the correct voltage levels required on the integrated controller. Detail design and evaluation of the flyback converter is beyond the scope of this thesis. The voltage ripple and voltage levels of the flyback outputs are checked however.

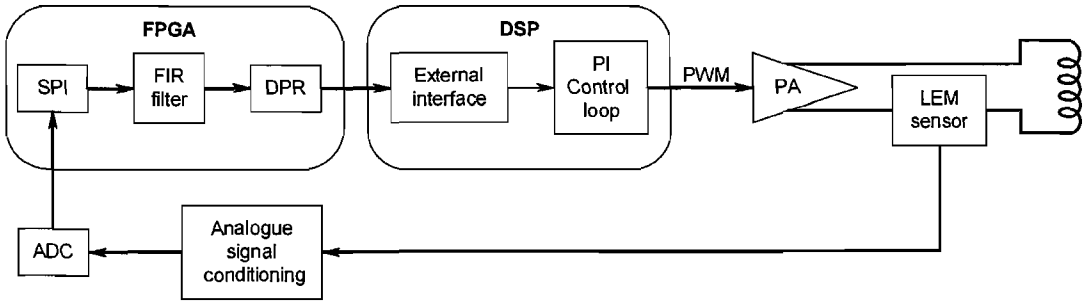


Figure 5.7: Power amplifier current control loop

Figures 5.8 and 5.9 shows the output voltages of a 5V and a 12V output of the flyback converter respectively. In both the signals a ripple of less than 30 mV is observed. The mean of the 5V output is approximately 4.98 V and 13.89 V for the 12 V output. The flyback converter has a switching frequency of 50 kHz that can be observed in the ripple voltage. It is worth mentioning that the switching of the flyback converter is not synchronised with any other signals on the integrated controller.

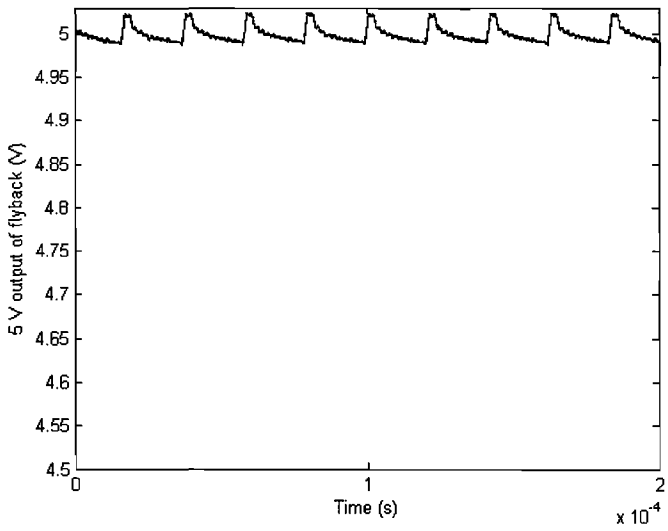


Figure 5.8: 5V output voltage of the flyback converter

5.2.3 Initial evaluation of power amplifier

At this stage of the evaluation process the DSP has successfully been programmed. A PWM signal is now verified to be present on the inputs of the drivers for the IGBTs of the power amplifier.

The power amplifier board is attached to the controller board and power is applied to the

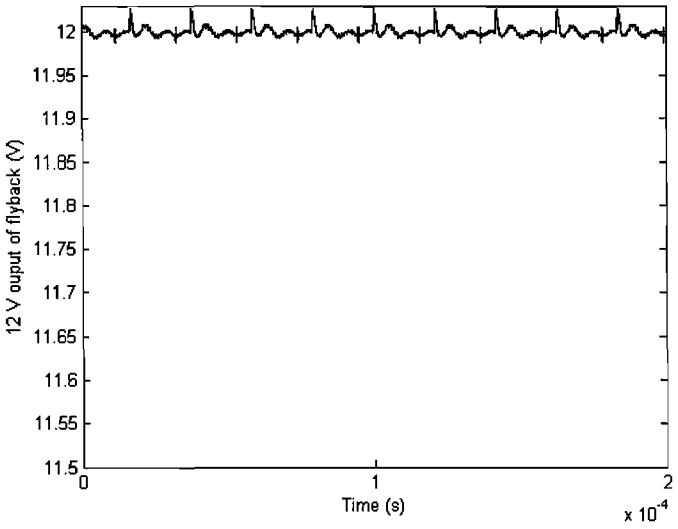


Figure 5.9: 12V output voltage of the flyback converter

bridges of the power amplifiers. The DSP is configured to drive each of the two 3-phase bridges in only 2-phase mode. The DSP PWM output signals are optimally connected for 3-phase operation. This unfortunately causes some restrictions to the DSP's PWM register configuration options. A 2-phase configuration can only be done as illustrated in Figure 5.10. This restricts the current to flow in only one direction through the load. This however does not pose a problem since suspending an AMB only requires positive current through the actuators.

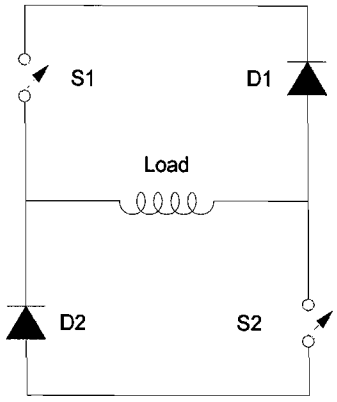


Figure 5.10: 2-phase configuration

The bridges of the amplifier are individually tested by applying an RL load to only one 2-phase bridge at a time. To resemble an actuator of an AMB, the load used for evaluation purposes is a laminated core inductor with 0.5 mm air gaps as illustrated in Figure 5.11. The the air gaps in the core will decrease the inductance but avoid core saturation. To verify that the core will not saturate the following is considered:

Under ideal conditions the reluctance of the air gap is dominant in comparison to the reluctance of the core material. When the core material saturates however, the reluctance of the core increases as a result of the relative permeability decreasing. This can be seen in (5.1) that shows the equations for calculating the reluctance of the air gap ($\Re_g$) and core material ($\Re_c$) respectively [27].

$$\Re_g = \frac{2(g+x)}{\mu_0 A_g}, \quad \Re_c = \frac{l_c}{\mu_0 \mu_r A_g} \tag{5.1}$$

$(g+x)$ represents the air gap, l_c the core path length, μ_0 the permeability of free space, μ_r the relative permeability of the core material and A_g the core area. If the core material saturates, the reluctance of the core becomes a larger factor in the total reluctance of the magnetic path [27]. According to (2.5) in section 2.1 if the relative permeability decreases, the current ripple will increase. By checking the current ripple through the load at different bias levels, it can be confirmed that the core does not saturate if the ripple amplitude stays constant.

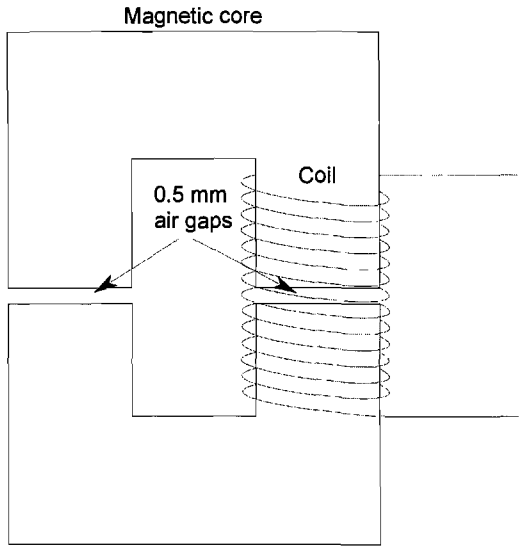


Figure 5.11: R-L load with core

Voltage and current are measured using a differential probe and a current clamp respectively connected to a digital oscilloscope. Figures 5.12 and 5.13 illustrate the current through and voltage across the load when a 50 V PWM signal with a 53 % duty cycle is applied to the 2-phase bridge. The ripple current amplitude stays relatively stable at 500 mA peak to peak for different bias levels, thus the air gap is sufficient to prevent core saturation.

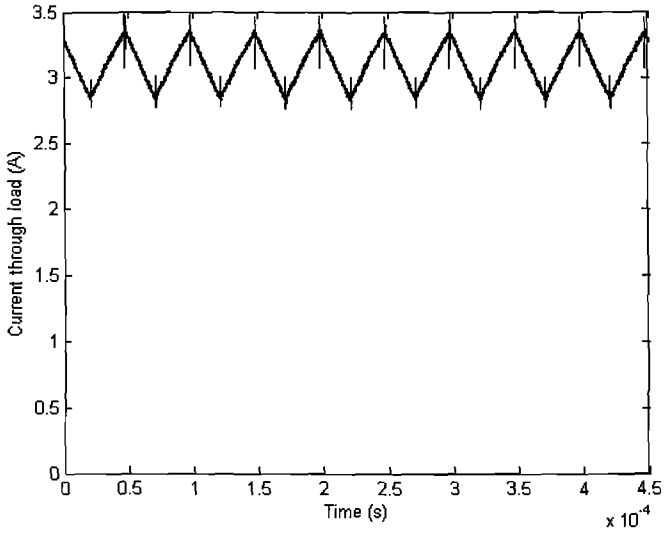


Figure 5.12: Ripple current through load

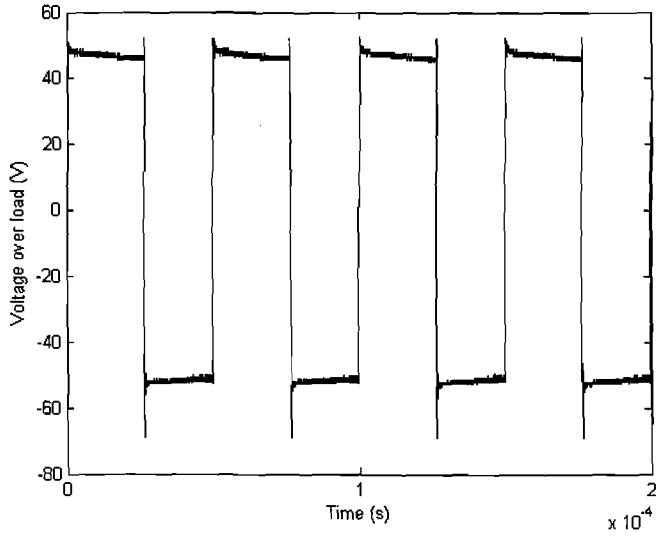


Figure 5.13: PWM voltage across load

5.2.4 Current limiting tests on power amplifiers

Once the power amplifiers are operational and produces expected voltages and currents under manual control, the over current and short circuit protection circuitry is tested. The same circuitry that limits the output current also protects against short circuits.

According to the specification in section 3.2 the amplifier's peak current should be limited to 15 A. To verify this the duty cycle is manually increased until the current peaks reach 15 A. Once the protection circuitry senses a current of 15 A it activates the shutdown pin on the drivers of

the IGBTs. Figure 5.14 illustrates the voltages on the shutdown pin of the drivers and the current through the load. The over-current circuitry activates pulse for pulse at approximately 14.5 A according to the measured results. The air gaps were removed when the over current protection was tested, which resulted in the core saturating and a current ripple of 2 A as seen in Figure 5.14.

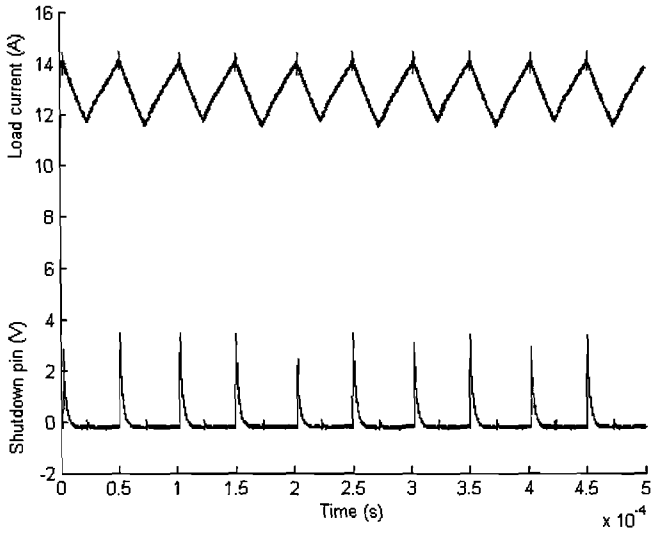


Figure 5.14: Voltage on shutdown pin and current through load.

After verifying that the over-current protection circuitry is working properly, short circuit tests can be performed. The test simply involves short circuiting the output of the power amplifier and measuring the peak current through the load. Table 5.1 shows the peak currents obtained from shorting the output at 10 V, 25 V and 50 V supply respectively. Figure 5.15 illustrates the current spikes when short circuiting the power amplifiers whilst a 25 V supply voltage is applied.

The current clamp can only measure up to 50 A accurately. To obtain the current at higher levels the data in Table 5.1 is extrapolated, resulting in 90 A peaks for 150 V and 173 A peaks for the maximum rated voltage of 310 V. The IGBTs and free wheeling diodes used can only manage 160 A and 170 A peak currents respectively. Although the short circuit protection is functioning well it still has its limitations and short circuiting of the power amplifiers should be avoided.

Table 5.1: Peak current spikes for short circuit test

Supply voltage (V)	**Peak current spike (A)**
10	16
25	26
50	37

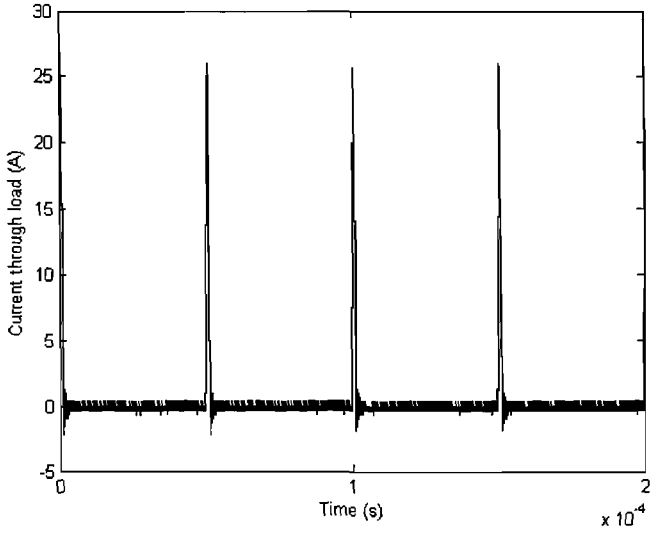


Figure 5.15: Current spikes when short circuiting the power amplifiers at a supply voltage of 25 V

5.2.5 ADC inputs

To perform closed loop control on the power amplifiers a feedback path is necessary for determining the error between the actual current and reference current.

The analogue PCB provides a signal conditioning path from the current sensors to two individual ADC inputs of the DSP (See Figure3.8 in section 3.2). This path will exclude the FPGA from the control loop. By including the FPGA in the control loop however (see Figure 5.7), more function capabilities of the integrated controller can be evaluated.

Figure 5.16 illustrates a plot of the scaled voltage at the input pin of an external ADC together with the actual current through the load. From the plot it can be seen that the two waveforms correspond well. The external ADCs has true differential bipolar inputs up to ± 10 V.

The FPGA is configured to interface with the ADCs, filter the digitized data and place it in DPR where the DSP can fetch the results as illustrated in Figure 5.6. The digitized value still needs scaling in the DSP. To obtain an equation for converting the ADC's digitized data to actual current, the digitized data is compared with the actual current at different levels a curve fit is performed on the data.

5.2.6 Power amplifier closed loop control

Before closed loop PI control can be implemented on a power amplifier, the proportional constant (K_p) needs to be determined to meet the power bandwidth and small signal bandwidth requirements. The load current is given by the transfer function in (5.2).

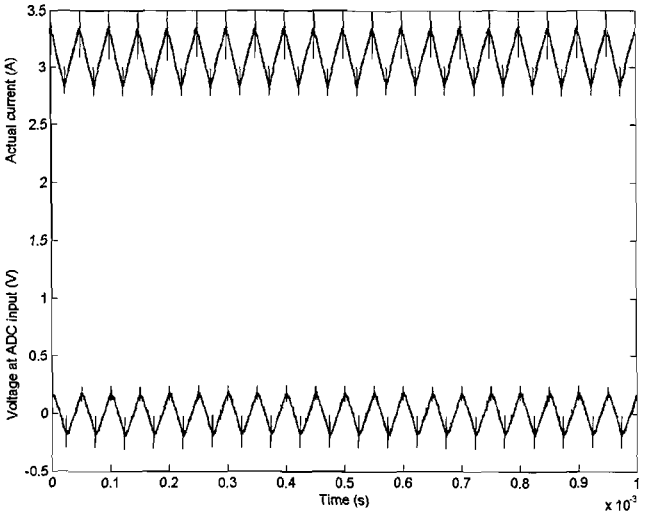


Figure 5.16: Voltage at ADC input pin and actual current through load

$$I(s) = \frac{V(s)}{sL + R} \tag{5.2}$$

where $V(s)$ is the load voltage and L and R are the inductance and resistance of the load respectively.

A simplified closed loop controlled amplifier model is presented in Figure 5.17.

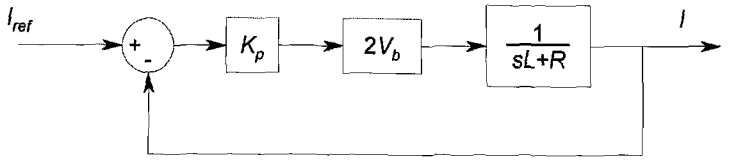


Figure 5.17: Power amplifier model

From the model in Figure 5.17 the transfer function of the power amplifier model is derived to be as given in (5.3)

$$I(s) = \frac{2K_P V_b / L}{s + \frac{R + 2K_P V_b}{L}} I_{ref}(s) \tag{5.3}$$

where K_P is the proportional gain of the PI control loop and V_b is the dc rail supply voltage of the 2-phase bridge. From the transfer function the small signal bandwidth can be derived as given by (5.4).

$$\omega_{bw} < \frac{R + 2K_p V_b}{L} \tag{5.4}$$

To use (5.4) the RL values of the load has to be known. Using an RLC analyser the load's RL values are measured at dc and found to be:

R = 0.1 Ω
L = 2.3 mH;

For the purpose of suspending an AMB the small signal bandwidth of the power amplifiers should be at least 2500 Hz. Using (5.4) the K_P value is determined to be 0.36. The integral gain (K_I) is chosen as 0.1.

Power bandwidth verification

The power bandwidth of hte power amplifiers is defined as the maximum frequency at which the amplifier can reach the full variation around the mid operating point [1]. For the case at hand this translates to the frequency where a current reference of $5sin\omega t$ can be followed around a operating point of 5 A. To achieve the slope of the sinusoidal reference should not exceed the slope of the ripple current. To ensure this the amplitude and frequency of the reference should be kept in check. To determine the power bandwidth the maximum derivative of a sinusoidal signal is set equal to the maximum achievable change in current as given by (5.5).

$$\max\left(\frac{d}{dt} A \sin \omega t\right) < \frac{V_b}{L} \tag{5.5}$$
$$\text{thus } A\omega < \frac{V_b}{L}$$

With A chosen as 5 A and V_b taken as 50 V the power bandwidth will be approximately 692 Hz.

Figures 5.18 and 5.19 show the 10 V peak to peak sinusoidal current reference and actual current at approximately 680 Hz and 760 Hz respectively. In both cases the actual current manages to follow the reference, leading to the conclusion that the power bandwidth as higher than the calculated 692 Hz.

The small signal bandwidth of the power amplifiers are now evaluated. Using (5.5) the maximum amplitude for a reference signal of 2500 Hz is calculated as 1.36 A, or 2.72 A peak

to peak. Figure 5.20 illustrates a sinusoidal reference at 1 kHz with a peak to peak current of 2 A. The actual current manages to follow the reference current as can be seen in the plot. To determine the small signal bandwidth of the power amplifier the frequency of the reference is increased until the actual current's amplitude is 3dB less than the current reference's amplitude. This happens at 2500 Hz as illustrated in Figure 5.21.

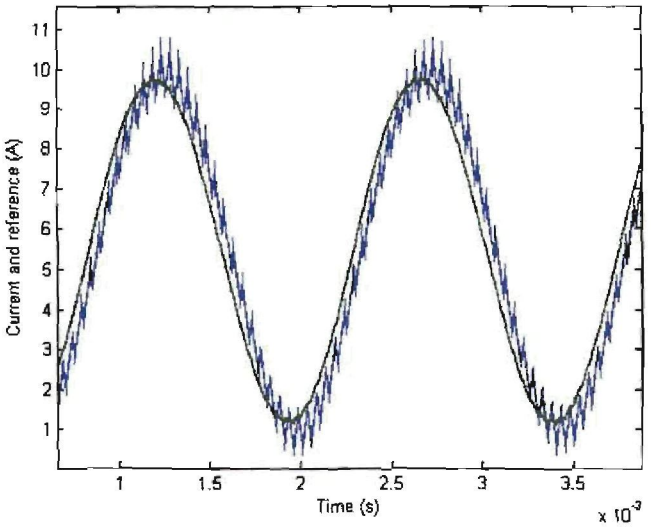


Figure 5.18: 680Hz sinusoidal current reference and actual current

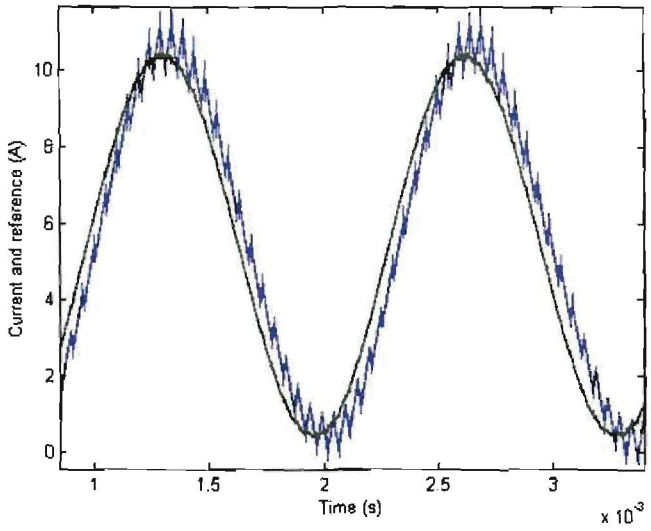


Figure 5.19: 10 V peak to peak 760Hz sinusoidal current reference and actual current

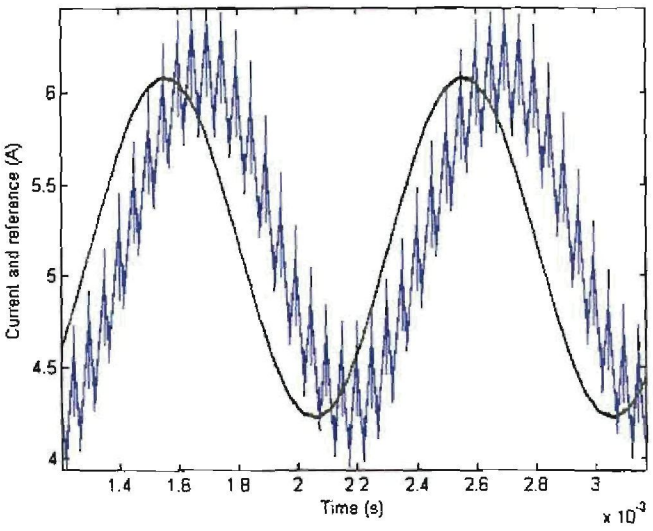


Figure 5.20: 2 A peak to peak 1000 Hz sinusoidal current reference and actual current

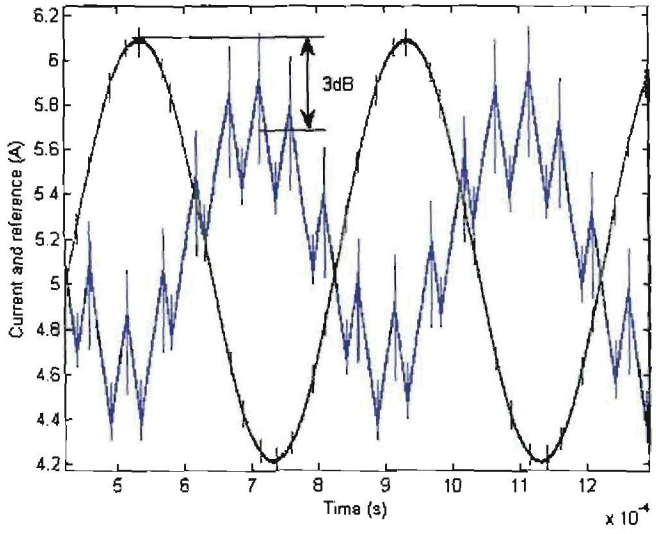


Figure 5.21: 2 A peak to peak 2500 Hz sinusoidal current reference and actual current

5.2.7 Algorithm evaluation

Practical measurements were taken to determine the amount of resources certain algorithms require on an embedded device. In this section the execution time of an finite impulse response (FIR) filter will be measured on both the DSP and FPGA, as well as the execution time of a PID control loop on the DSP.

The specifications of the lowpass FIR filter that was implemented on the DSP is listed in table 5.2. Figure 5.22 illustrates the phase and magnitude plots of the filter.

Table 5.2: FIR specifications

Order	Sampling frequency (f_s)	Passband frequency (f_{pass})
50	20 kHz	2.5 kHz

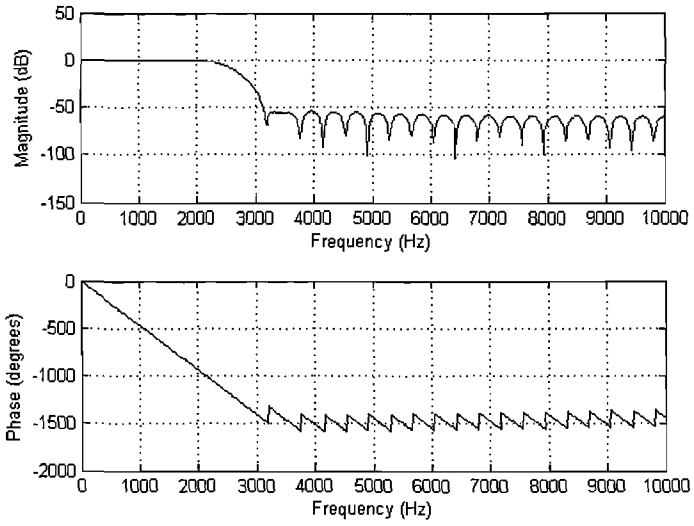


Figure 5.22: Magnitude and phase plot of FIR filter implemented in DSP

Measurement of the execution speed is done by forcing a pin of the embedded device high just before the algorithm starts executing, and forcing it low again immediately after the algorithm finishes. Figure 5.23 shows the execution graph for the FIR filter. The pulses are 600 ns wide and spaced 50 µs apart. The FIR filter thus takes 600 ns to filter a 16-bit value at a sampling frequency correlating with the specification of 20 kHz. One instruction cycle takes approximately 6.67 ns on the DSP. The FIR filter thus takes approximately 90 instruction cycles to execute.

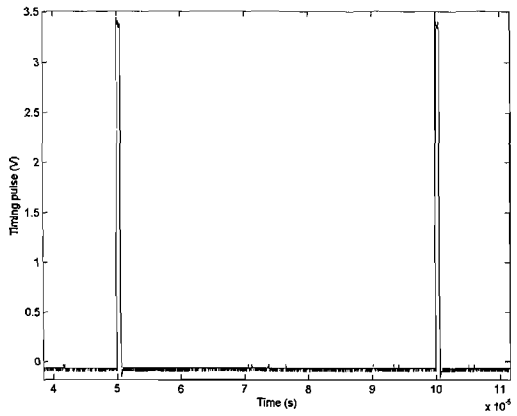


Figure 5.23: Execution time of FIR filter on DSP

The execution time of a PID control loop on the DSP is illustrated in Figure 5.24. It takes the DSP approximately 270 ns to execute a PID control loop, equating to about 70 instruction cycles.

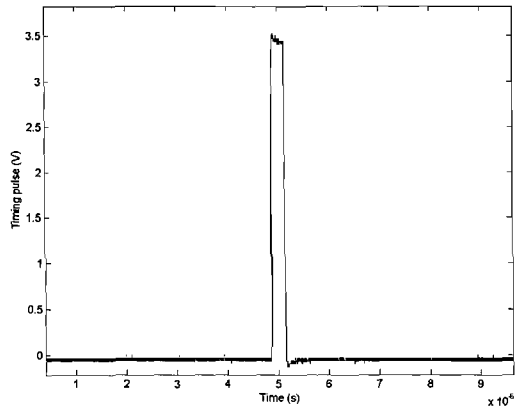


Figure 5.24: Execution time of PID control on DSP

The same filter was implemented on the FPGA, except the sampling frequency is 800 kHz. The magnitude and phase plots of the filter implemented on the FPGA is illustrated in Figures 5.25 and 5.26 respectively. According to the phase plot only about 6° phase shift is present at 2.5 kHz which results in about 33 μs time delay.

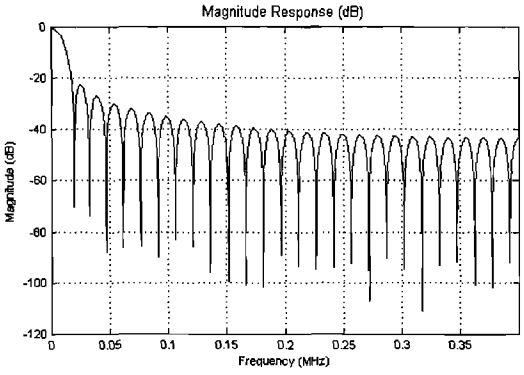


Figure 5.25: Magnitude plot of FIR filter implemented in FPGA

Table 5.3 lists the resources consumed on the FPGA by the FIR filter. The amount of configurable slices available on this specific FPGA is 4656. Only about 2 % is used by the FIR filter.

Table 5.3: Resources consumed by FIR filter

Slices	Multipliers	Block memory
100	1	1

Illustrated in Figure 5.27 is the execution graph for the FIR filter on the FPGA. It takes the

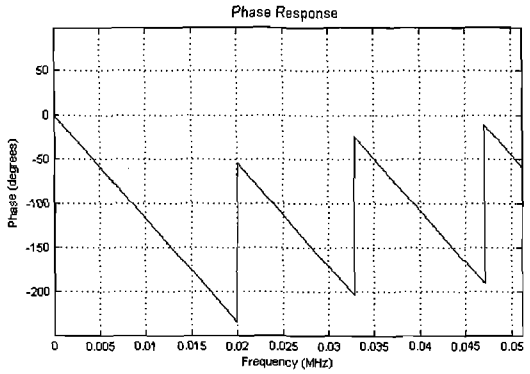


Figure 5.26: Phase plot of FIR filter implemented in FPGA

FPGA approximately 60 ns to execute. The time of 60 ns can actually be halved since this specific implementation of the FIR filters two 16-bit values in the 60 ns. Thus it takes only 30 ns to filter a single 16-bit value on the FPGA.

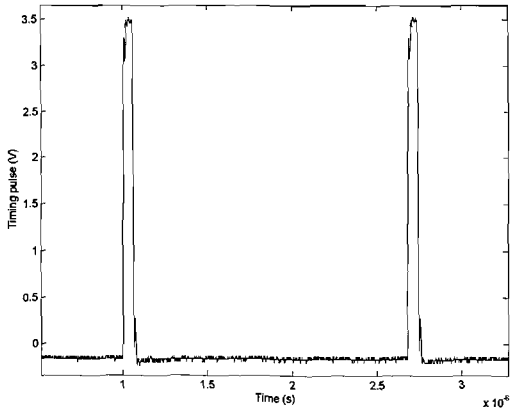


Figure 5.27: Execution time of FIR filter on FPGA

A 256 point FFT was implemented on the FPGA. Figure 5.28 illustrates the execution graph for the FFT on the FPGA. The FFT takes only 11 μs to execute and does so every 50 μs. It executes every 50 μs because this specific algorithm moves the window of data used in the FPGA forward in 50 μs intervals. The window of data is basically 256 data points sampled at 1 Msps. This is equivalent to one data point every 1 μs. If the window of data is moved on 50 μs, 50 new data points are acquired. 50 new data points are thus shifted into a 256 point buffer while the 50 oldest data points are shifted out and discarded.

Table 5.4 shows the amount of resources the 256 point FFT consumes on the FPGA. It already takes up 56 % of the slices, 90 % of the multipliers and 55 % of the memory available on the FPGA. Only one instantiation can be implemented on the FPGA, but due to the speed at which it executes, multiple data sets can be transformed in a very short time using the same FFT instantiation.

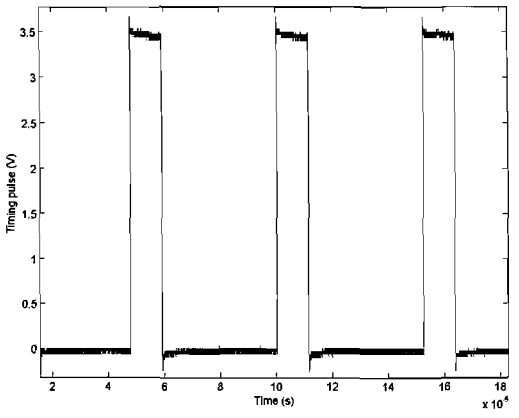


Figure 5.28: Execution time of FFT on FPGA

Table 5.4: Resources consumed by FFT

Slices	Multipliers	Block memory
2616	18	11

5.2.8 Conclusion

This concludes the evaluations on the integrated controller. The most fundamental functionality has been evaluated which includes converting analogue signals to digital data, processing the data and driving the power amplifiers. The building blocks have now been laid for further expansion of algorithms for self sensing investigations. In Chapter 6 to follow, more thorough conclusions and recommendations will be given.

Chapter 6

Conclusion and recommendations

Chapter 6 starts off by discussing the results obtained from evaluating the power amplifiers. Algorithm evaluations is discussed next where it is concluded that the embedded devices offer enough power and resources for the implementation and evaluation of self-sensing. Work to be done in the future on the integrated controller is proposed. A final conclusion is drawn in the last paragraph.

6.1 Power amplifiers

The Nyquist theorem states that the sampling frequency should be at least twice the sampled signal's frequency [9]. A good rule of thumb however is to sample a signal at five times its frequency [24]. The bandwidth of the applicable McTronx AMB model is 500 Hz. In other words the maximum rate at which the rotor position can change is 500 Hz. The bandwidth of the power amplifiers when using closed loop control is 2.5 kHz; five times higher than the AMB system bandwidth. This is a favourable result and thus the power amplifiers are suitable for suspending the AMB. The control loop was designed for a bandwidth of 2.5 kHz, but by altering the design it might be possible to increase the bandwidth of the power amplifiers for other applications of the integrated controller.

The current through the load, illustrated in Figure 5.12 exhibit an almost perfect triangular current ripple with very little distortion or ringing. This is favourable, especially for the purpose of using the current signal for extracting rotor position information. Another pleasing evaluation result is the excellent representation of the current signal at the ADC inputs illustrated in Figure 5.16. The signal at the ADC inputs is thus an accurate representation of the actual current, making it suitable for self-sensing purposes.

6.2 Algorithms

The resources utilized on the FPGA are measured by comparing the number of gates, RAM and multipliers an algorithm instantiation consumes on the FPGA, to the amount of gates, RAM and multipliers available on the FPGA. The DSP resource utilization is measured in terms of the number of instruction cycles an algorithm would need to execute. The RAM and ROM the algorithms on the DSP consume are so small in comparison with the amount of RAM and ROM available on this specific DSP, that it is not meaningful to evaluate.

Table 6.1 summarizes the amount of resources the FIR filter and FFT instantiation on the FPGA consumes. The FFT consumes the largest part of the resources which is more than 50 %. Only one FFT can thus be instantiated on the FPGA. According to table 4.4 in Section 4.1.2 eight FIR filters and a FFT transform on two sets of data are required in a self-sensing algorithm. Because of the speed of execution of the FFT, the same FFT instantiation can be used to transform two separate sets of input data within a 50 µs time period. The filter instantiation on the FPGA can filter multiple input signals. Thus the eight FIR filters required by the self-sensing algorithm does not necessarily imply eight instantiations of filters on the FPGA. The FPGA thus still offers enough resources for several algorithm instantiations.

Table 6.1: Resources consumed on FPGA according to evaluation results

	Slices	**Multipliers**	**Block memory**
FIR	2%	5%	5%
FFT	52%	55%	90%
Total	54%	60%	95%

Table 6.2 summarizes the amount of cycles three PID loops and four FIR filters would require on the DSP. Three PID loops are chosen because two PI loops are required for the two 3-phase power amplifiers and one PID loop is required for the position control of the AMB.

Table 6.2: Resources consumed on DSP according to evaluation results

	Instruction cycles	**Amount required**	**Total**	**Utilization**[1]
PID	70	3	210	2.8%
FIR	90	4	360	4.8%
			570	7.6%

[1] The percentage of cycles utilized by an algorithm out of the 7496 cycles available in a 50 µs time period.

A full self-sensing algorithm has not yet been implemented on the embedded devices and thus the exact number of filters on each embedded device has yet to be determined. The four filters mentioned in table 6.2 is just a chosen number.

From the table it can be seen that only 7.6% of the amount of instruction cycles available in 50 μs are used by these algorithms. It has to be noted however that a lot of other processes are also running on the DSP, including scaling and conversion of input data to correct formats, updating of PWM signals, timer interrupt functions etc. These processes all require instruction cycles. The DSP and FPGA will each have its share of algorithms to execute. According to this first order resource budgeting, both devices offer enough resources for complex algorithm implementation.

6.3 Integrated system

Integrating digital, analogue and power amplifiers into a piggy-backed system has poses some unique design issues and requires insight when it comes to the routing and grounding of such a wide spectrum of signals. Thanks to the collaborative development of the integrated controller with an industry partner the integrated system passed the general evaluation with flying colours. From the evaluation results it is clear that the integrated system works well.

6.4 Future work

Here follows a list of further work to be done using the integrated controller:

AMB suspension The ground work has been laid for the suspension of an AMB in one degree of freedom using the integrated controller. This suspension will still require the input of a position sensor but will provide another intermediate step before self-sensing can be implemented.

Evaluate communication interfaces The communication interfaces on the integrated controller have not been evaluated. This includes RS485, USB and RS232. The RS485 and USB driver circuitry are directly connected to the FPGA. Instantiations for communication interfaces thus have to be coded onto the FPGA. The RS232 driver circuitry is connected to the DSP. The firmware on the DSP has to be extended to allow serial interfacing with the DSP.

External RAM A logic interface with the external RAM needs to be instantiated in the FPGA to grant both the DSP and the FPGA read and write access to the external RAM.

Further evaluation of an FFT algorithm The FFT algorithm needs to be verified. Only an instantiation of the FFT has been implemented on the FPGA. The results of the transform need to be extracted to a PC where it can be analysed with a mathematical package such as MATLAB®. This will require writing the results of the FFT to external RAM and then

extracting the data to a PC via one of the communication interfaces (RS485, USB, RS232). The data will need to be placed in RAM first because the communication interfaces are too slow to allow real time exporting of data to a PC.

Further evaluation of analogue circuitry The analogue PCB contain switched capacitor filters. These filters are for self-sensing purposes and has been bypassed for the evaluation process. The output of these filters need to be evaluated first before self-sensing algorithms can be implemented.

Self sensing algorithm implementation The integrated controller's ultimate purpose is the implementation of self-sensing algorithms. This will test a large portion of the integrated controller's full potential.

6.5 Conclusion

Although the development of the integrated controller was a somewhat risky and expensive leap into a lot of unknowns, it proved to be a success. The integrated controller now provides an excellent platform for not only self-sensing investigations, but also many other actuator or motor control schemes. Indispensable insight, experience and technical skills were acquired in the development process of the integrated controller that will prove extremely valuable for future projects in the McTronX research group.

Bibliography

[1] G. Schweitzer, H. Bleuler, and A. Traxler, *Active Magnetic Bearing Basics: Properties and Applications of Active Magnetic Bearings*. Zrich: Author's Reprint, 2003.

[2] L. Shi, L. Zhao, G. Yang, H. Gu, X. Diao, and S. Yu, "Design and experiments of the active magnetic bearing system for the HTR-10," in *Second international topical meeting on high temperature reactor technology*, no. D04. Beijing, China: Institute of Nuclear and New Energy Technology, September 22–24, 2004, p. 3.

[3] A. Schammass, "A self-sensing active magnetic bearing: Modulation approach," Ph.D. dissertation, July 2003.

[4] "RS485 and RS422," B&B Electronics, Ottawa IL, Appl. Note, October 1997.

[5] R. Kliger and S. Klark, "*i*coupler® isolation in CAN bus applications," Analog Devices, Norwood, MA, Appl. Note AN-770, 2005.

[6] "Interface circuits for TIA/EIA-485 (rs485)," Texas Instraments, Design Notes, June 2002, literature number: SLLA036B.

[7] K. Arnold01, *Emedded controller hardware design*, ser. Embedded Technology. USA: LLH Technology Publishing, 2001.

[8] T. Williams, *EMC for product designers*, 3rd ed. Oxford: Newnes, 2001.

[9] E. C. Ifeachor and B. W. Jervis, *Digital signal processing: A practical approach*, 2nd ed. New York: Prentice Hall, 2002.

[10] (2007, July) Is DSP right for you? Texas Instraments. [Online]. Available: http://focus.ti.com/dsp/docs/dspsupporto.tsp?sectionId=4&tabId=1443

[11] V. A. Pedroni, *Circuit design with VHDL*. Cambridge, Massachusetts: MIT press, 2004.

[12] (2007, July) Getting started with FPGAs. Xilinx. [Online]. Available: http://www.xilinx.com/company/gettingstarted/index.htm

[13] P. L. Douglas, *VHDL: Programming by example*, 4th ed. New York: McGraw-Hill, 2002.

[14] T. Hill, "The benefits of FPGA coprocessing," Xilinx, Tech. Feature, 2006.

[15] P. Ekas and B. Jentz, "Developing and integrating FPGA coprocessor," Altera, Tech. Feature, 2003.

[16] G. Becke, C. Bogert, S. Corrigan, M. Dehmelt, Frank Feulner, C. Gonzalez, M. Groenebaum, F. Kabir, A. Kacprzak, C. Kinnaird, and J. Zipperer, "Comparing bus solutions," Texas Instruments, Appl. Report SLLA067A, February 2004.

[17] M. Soltero, J. Zhang, and C. Cockrill, "422 and 485 standards overview and system configurations," Texas Instruments, Tech. Rep. SLLA070C, June 2002.

[18] Dictionary.com unabridged (v 1.1). Random House Inc. [Online]. Available: http://dictionary.reference.com/browse/system

[19] B. S. Blanchard and W. J. Fabrycky, *Systems engineering and analysis*, 4th ed. New Jersey: Prentice Hall, 2006.

[20] *Systems Engineering*, Electronic Industries Alliance, Interim Std. EIA/IS 632, 1994.

[21] *Standards for Application and Management of the Systems Engineers Process*, Institute of Electrical and Electronics Engineers Std. IEEE P1220, 1994.

[22] "An overview of switch mode power supplies," Philips semiconductors, Appl. Note AN120, December 1988.

[23] *FFT library: Module user's guide*, Texas Instruments, May 2002.

[24] C. L. Phillips and H. T. Nagle, *Digital control system analysis and design*, 3rd ed. Upper Saddle River, New Jersey: Prentice Hall, 1995.

[25] *Spartan-3E FPGA family: Complete data sheet*, Xilinx®, November 2006, literature number: DS312.

[26] G. Gonzalez, *Microwave transistor amplifiers: Analysis and design*, 2nd ed. New Jersey: Prentice Hall, 1997, ch. One, p. 9.

[27] M. D. Noh and E. H. Maslen, "Self-sensing magnetic bearings (part II) - Effects of Saturation," in *Proceedings of the 5th International Symposium on Magnetic Bearings*, Kanazawa, Japan, August 1996, pp. 1 – 3.

APPENDIX

Appendix A: System specification

Subsystem development specification

Integrated Controller design for an Active Magnetic Bearing

DOCUMENT IDENTIFICATION

Project Title:	Masters degree project
Document Number:	NWU-JJVR-2006-001-02C
System / Subsystem Title:	Integrated controller for an Active Magnetic Bearing
Document Issue Date:	2006-06-19
Client:	Prof. G van Schoor

ORIGINATION AND APPROVAL

Checked by party	Individual name	Signature	Date
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Technical Approval:	André Niemann		
Project Manager:	Eugén Ranft		

ACCEPTANCE

Checked by	Name	Signature	Date
Accepted by:			

DISTRIBUTION LIST

Company	Person name	Date
University of the North West	André Niemann	
University of the North West	Eugen Ranft	
Denel		

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Level	Description	Applicable level
1	Strictly confidential – not to be distributed	
2	Company confidential – distributed inside company	
3	Client confidential – distributed to limited clients and contractors	X
4	Public domain – distributed freely	

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DEFINITION OF TERMS AND ACRONYMS

AMB	Active Magnetic Bearing
ADC	Analogue to Digital Converter
I/O	Input Output
PCB	Printed Circuit Board
JTAG	Joint Test Action Group
MBMC	Magnetic Bearing
NWU	North West University
PWM	Pulse Width Modulation

Controller circuitry	Digital and analogue circuitry that together forms part of the controller for an Active Magnetic Bearing.
Integrated controller	The controller integrated with two power amplifiers.

1. DEVELOPMENT SPECIFICATION SCOPE

1.1 IDENTIFICATION

This specification establishes the performance, design, development, and test requirements for a integrated controller for an active magnetic bearing.

1.2 SYSTEM OVERVIEW

The controller is part of the complete architecture of an active magnetic bearing. Figure 1-1 illustrates a high level architecture concept for an active magnetic bearing (AMB). Two power amplifiers are needed for the suspension of a rotor in one degree of freedom. One controller will be integrated for a degree of freedom; in other words one controller is to be integrated with two power amplifiers.

The controllers shall be able to transfer data between each other and a main controller via a digital communication link. The main controller requirements are not included in this specification. The controllers themselves shall also be able to transfer data to and from a PC.

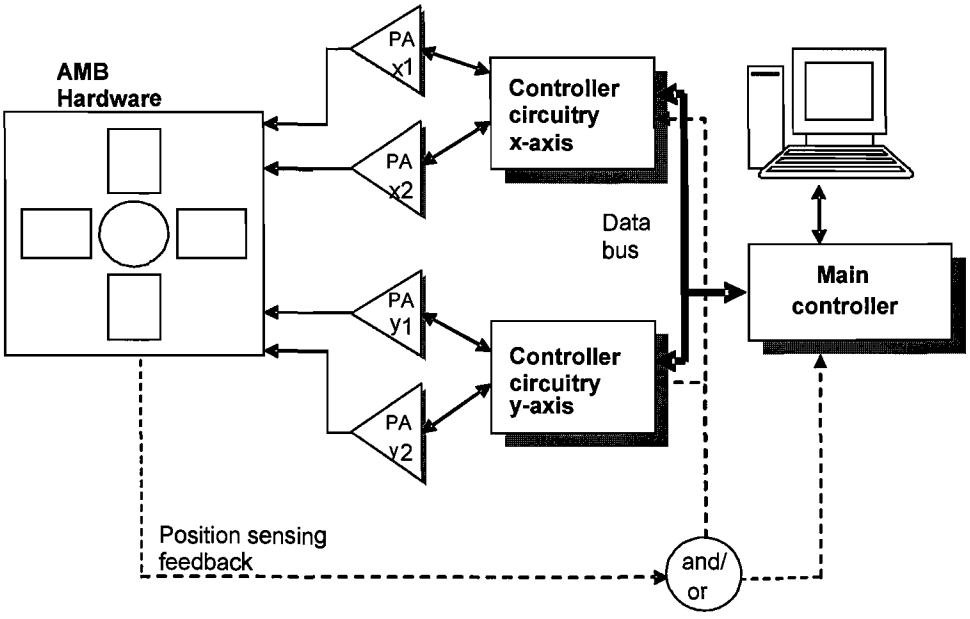

FIGURE 1-1 AMB SYSTEM CONCEPT

1.2.1 SUB SYSTEM: CONTROLLER INTEGRATED WITH TWO POWER AMPLIFIERS

Figure 1-2 illustrates the integrated controller for the single axis or one degree of freedom control of the AMB. The figure also illustrates the external inputs and outputs that will interface with integrated controller.

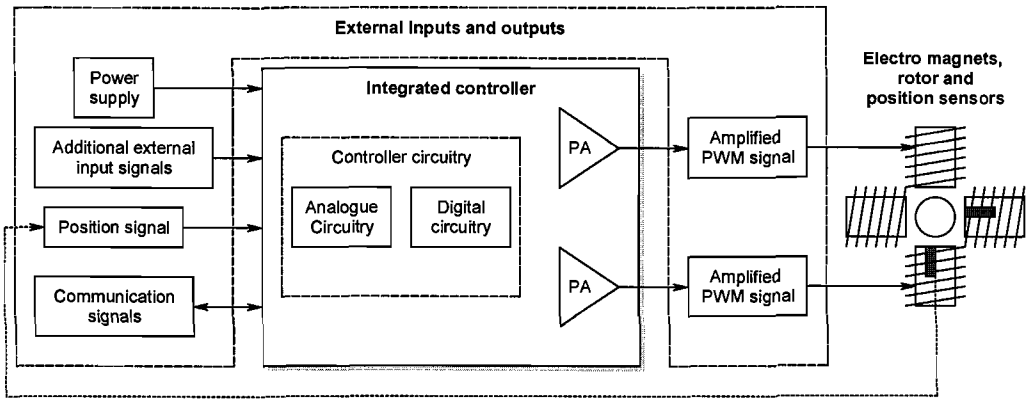

FIGURE 1-2 SUB SYSTEM: INTEGRATED CONTROLLER

1.3 DOCUMENT OVERVIEW

This development specification has been produced during the system preliminary design phase.

Before completion of the critical design review for the hardware configuration items (HWCI's), this specification will establish part of the functional baseline and subject to change using a change control procedures and a configuration management plan.

2. INTEGRATED CONTROLLER REQUIREMENTS

2.1 INTEGRATED CONTROLLER FUNCTIONAL ARCHITECTURE AND UNITS

2.1.1 SYSTEM FUNCTIONAL ARCHITECTURE AND UNITS

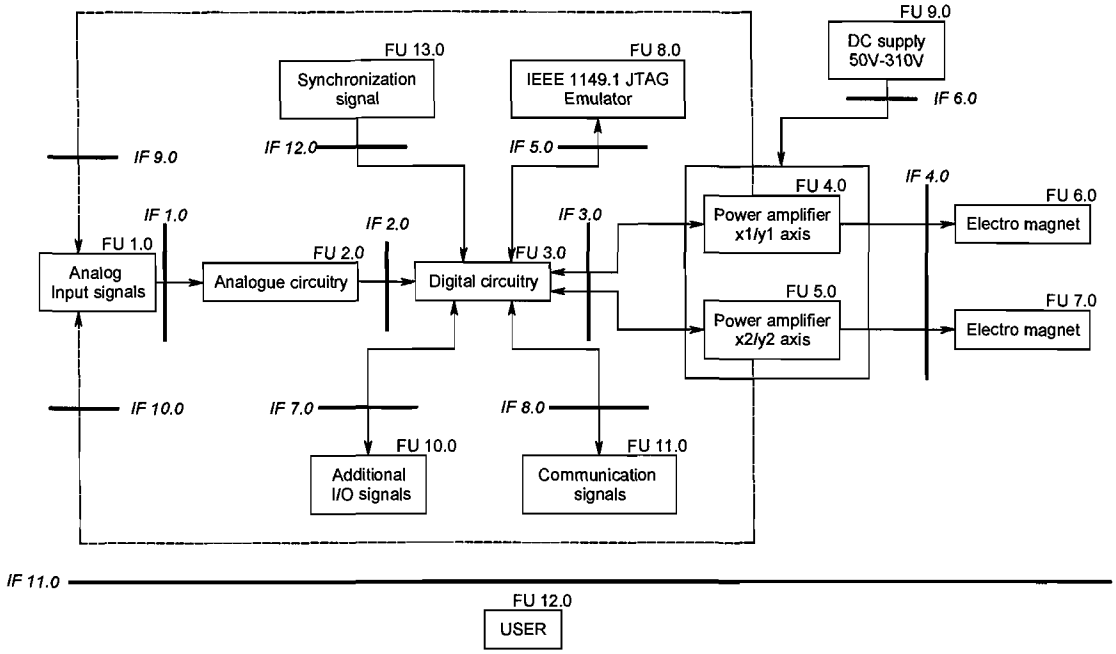

FIGURE 2-1 FUNCTIONAL ARCHITECTURE OF AN AMB SYSTEM

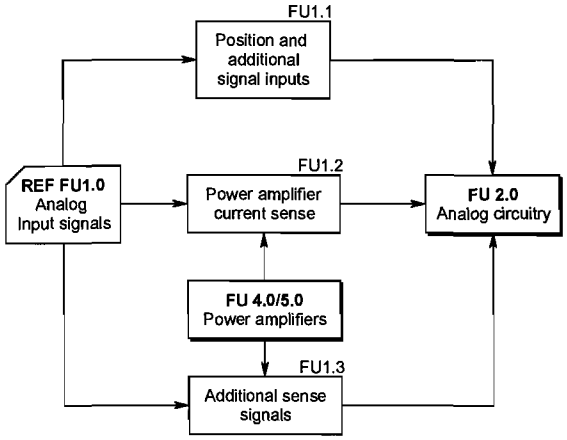

FIGURE 2-2 INPUT SIGNALS TO DIGITAL CONTROLLER

2.1.1.1 FUNCTIONAL UNIT 1.0: INPUT SIGNALS

The analogue input signals that will be input the analogue circuitry are the following:

TABLE 2-1INPUT SIGNALS TO ANALOGUE CIRCUITRY

Number of inputs	Type	Range	Input to:	Signal obtained from	Bandwidth
1	Position signal	0 V to -24 V	Main embedded device	External	0 to 2 kHz
3	Additional external signals	N/A	Main embedded device	External	0 to 2 kHz
2	Power amp current sense	Depends on sensor used	Main embedded device	PA	0 to 2 kHz
4	Additional sense circuitry	+-10 V	FPGA	PA	0 to 500 kHz

2.1.1.2 FUNCTIONAL UNIT 2.0: ANALOGUE CIRCUITRY

A separate PCB shall be manufactured for the analogue circuitry. The PCB containing the analogue circuitry shall be able to plug into the PCB containing the digital circuitry. The analogue circuitry will thus be "piggy backed" on the digital circuitry.

An area shall be provided on the PCB for the implementation of in-house designed filters, buffers and circuitry. The in-house analogue circuits will be designed for the following inputs:

1. Position signals;
2. Additional external signals.
3. Power amp current sense;
4. Additional sense circuitry.

The analogue circuitry will perform function F2.8.1 as illustrated in paragraph 2.3.

2.1.1.3 FUNCTIONAL UNIT 3.0: DIGITAL CIRCUITRY

A separate PCB shall be manufactured for the digital circuitry. The PCB containing the digital circuitry shall be able to plug into the PCB containing the power amplifiers circuitry. The digital circuitry will thus be "piggy backed" on the power amplifier circuitry.

The Digital circuitry will perform functions F2.8.2 through F2.8.7.

2.1.1.4 FUNCTIONAL UNIT 4.0 AND 5.0: POWER AMPLIFIERS

The power amplifiers will perform functions F6.0 and F7.0.

2.1.1.5 FUNCTIONAL UNIT 6.0 AND 7.0: ELECTRO MAGNETS

The electromagnets perform function F8.0.

2.1.1.6 FUNCTIONAL UNIT 8.0: IEEE 1149.1 JTAG EMULATOR

The Emulator will be used for functions F2.2, F2.7 and F2.9.

2.1.1.7 FUNCTIONAL UNIT 9.0: DC SUPPLY 50V-310V

In house DC supply units shall be used for powering amplifiers.

2.1.1.8 FUNCTIONAL UNIT 10.0: ADDITIONAL INPUT/OUTPUT SIGNALS

The additional signals refer to any other signals, not mentioned in this specification, that need to interface with the I/O ports of the embedded devices in the course of using the integrated controller.

The additional input signals are used for function F2.8.7.

2.1.1.9 FUNCTIONAL UNIT 11.0: COMMUNICATION SIGNAL

The communication signal will be used in function F2.8.6.

2.1.1.10 FUNCTIONAL UNIT 12.0: USER

The user will perform functions F2.5 to F2.5 and F2.9.

2.1.1.11 FUNCTIONAL UNIT 13.0: SYNCHRONIZATION SIGNAL

An embedded device should be able to synchronize with other external embedded devices by means of a synchronization signal.

The synchronization signal will perform function F2.8.8.

2.1.2 ANALOGUE CIRCUITRY FUNCTIONAL ARCHITECTURE AND UNITS

The analogue circuitry shall be electrically shielded.

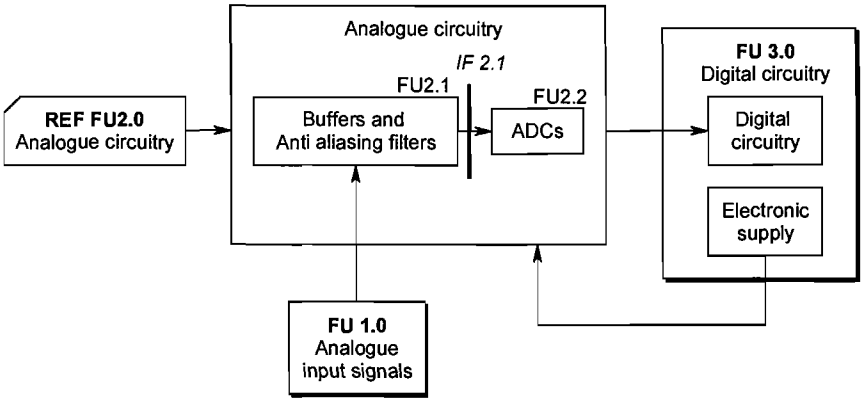

FIGURE 2-3 ANALOGUE CIRCUITRY FUNCTIONAL ARCHITECTURE

2.1.2.1 FUNCTIONAL UNIT 2.1: BUFFERS AND ANTI ALIASING FILTERS

The buffers anti aliasing filters will perform function F2.8.1.

2.1.2.2 FUNCTIONAL UNIT 2.2: ADCS

All ADC pins on the main embedded device shall be made available. 6 ADCs shall be available on the analogue circuitry PCB and 10 ADCs on the I/O expansion area.

Four AD7322 external ADCs shall interface with secondary embedded device (FPGA).

Refer to paragraph 2.3.3.2.

The ADCs will perform function F2.8.2.

2.1.3 DIGITAL CIRCUITRY FUNCTIONAL ARCHITECTURE AND UNITS

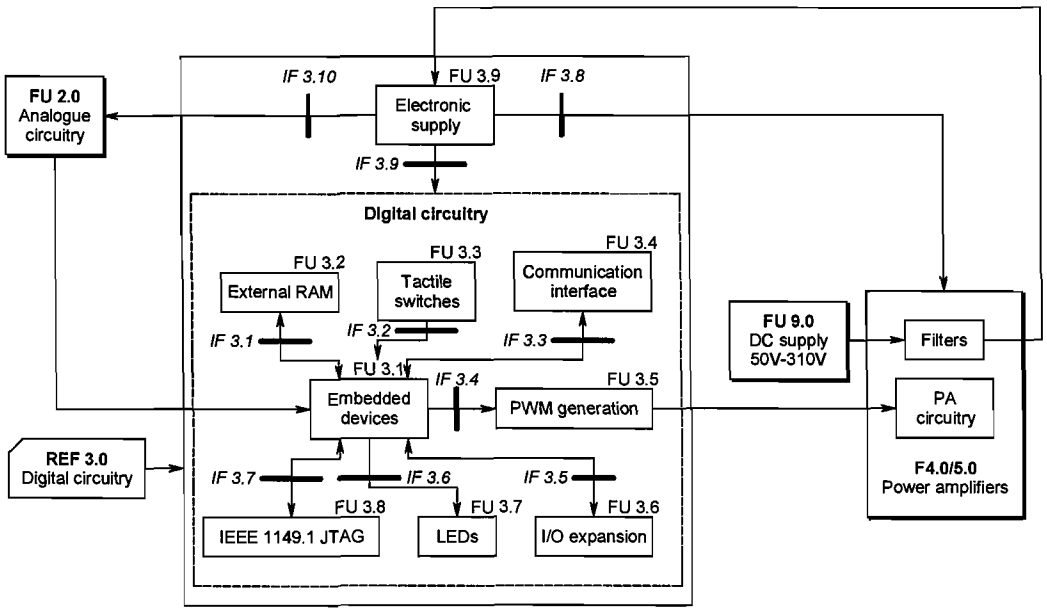

FIGURE 2-4 DIGITAL CIRCUITRY FUNCTIONAL ARCHITECTURE

2.1.3.1 FUNCTIONAL UNIT 3.1: EMBEDDED DEVICES

Two embedded devices shall be implemented on the digital circuitry PCB. A main embedded device (TMS320F2812) and a co-embedded device (Spartan 3E FPGA XC3S500E). The embedded devices shall be able to communicate with each other.

The embedded devices will perform function F2.8.4.

2.1.3.2 FUNCTIONAL UNIT 3.2: EXTERNAL RAM

The main embedded device shall interface with 512k x 16 SRAM. For debugging purposes firmware will be loaded in external RAM. After successful debugging the firmware will be loaded to flash memory. RAM will also be used for data logging purposes.

2.1.3.3 FUNCTIONAL UNIT 3.3: TACTILE SWITHCHES

5 switches shall be interfaced with the embedded devices to provide the user with tactile interfacing.

2.1.3.4 FUNCTIONAL UNIT 3.4: COMMUNICATION INTERFACE

Two appropriate communication line driver devices shall be interfaced with the DSP.

The Communication interface will perform function F2.8.6

2.1.3.5 FUNCTIONAL UNIT 3.5: PWM GENERATION

The user shall be able to choose if PWM signals are generated from main embedded device or slave embedded device.

The PWM generation will perform function F2.8.

2.1.3.6 FUNCTIONAL UNIT 3.6: I/O EXPANSION

An expansion area will be provided on the PCB that grants access to appropriate pins of both the embedded devices. Both analogue and digital pins of the main embedded device should be made available. Access to digital and analogue pins should be provided on separate areas.

The I/O expansion will perform functions F2.8.7

2.1.3.7 FUNCTIONAL UNIT 3.7: LEDS

6 LEDS (3 green and 3 red) shall be interfaced with general purpose I/O pins of the main embedded device to provide a visual interface to the user.

2.1.3.8 FUNCTIONAL UNIT 3.8: IEEE 1149.1 JTAG

The JTAG interface will be used for functions F2.2, F2.7 and F2.9.

2.1.3.9 FUNCTIONAL UNIT 3.9: ELECTRONIC SUPPLY

A fly-back converter shall be designed to provide devices with their supply voltages.

2.1.4 POWER AMPLIFIERS CIRCUITRY FUNCTIONAL ARCHITECTURE AND UNITS

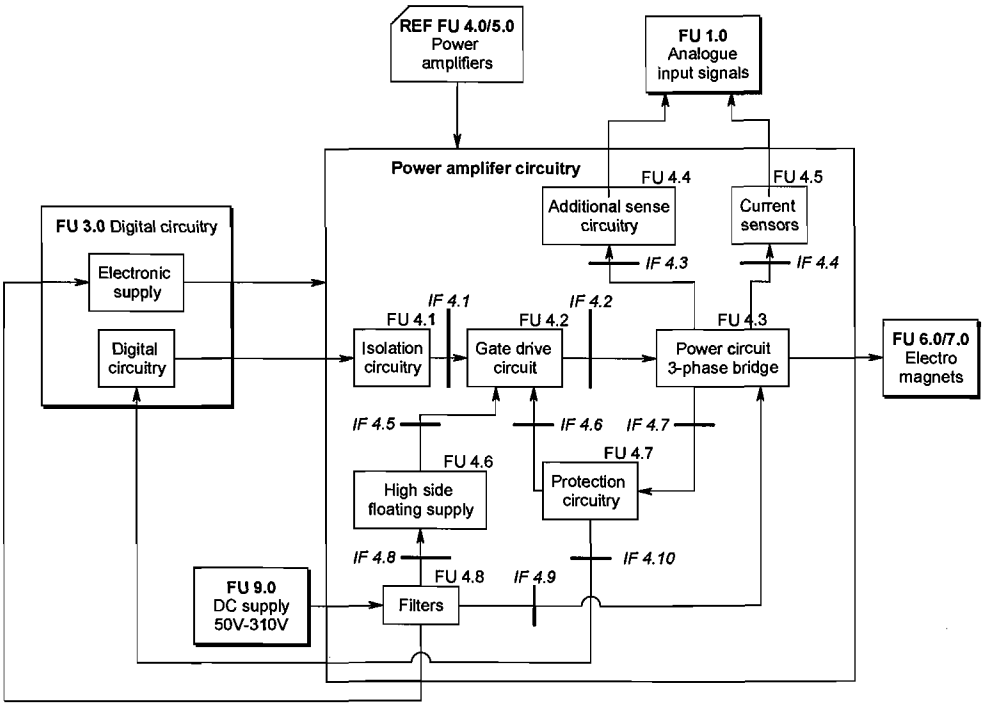

FIGURE 2-5 POWER AMPLIFIERS CIRCUITRY FUNCTIONAL ARCHITECTURE

2.1.4.1 FUNCTIONAL UNIT 4.1: ISOLATION CIRCUITRY

PWM control signals should be optically isolated.

The Isolation circuitry will perform function F6.1.

2.1.4.2 FUNCTIONAL UNIT 4.2: GATE DRIVE CIRCUIT

An adequate gate driver shall be used to drive the 3-phase power circuit.

The Gate drive circuit will perform function F6.2.

2.1.4.3 FUNCTIONAL UNIT 4.3: POWER CIRCUIT: 3-PHASE BRIDGE

Appropriate switching devices shall be used for the 3-phase bridge.

The 3-phase bridge will perform function F6.3.

2.1.4.4 FUNCTIONAL UNIT 4.4: ADDITIONAL SENSE CIRCUITRY

Additional sense circuitry shall use isolated measurement techniques to sense output voltage and current.

Two techniques for voltage sensing shall be implemented on the power amplifier circuitry. One technique shall utilize voltage divider resistors. The other technique shall utilize a voltage transformer. Three connectors shall be put on the power amplifier circuitry for interfacing with the analogue circuitry. Only two cables shall be utilized for connecting the additional sensing circuitry with the analogue circuitry: one for connecting the voltage sensing and the other for the current sensing. The user shall be able to connect the voltage sense cable to either one of the voltage sense connectors.

Connector 1: Voltage sensing utilizing voltage transformer;

Connector 2: Voltage sensing utilizing divider resistors;

Connector 3: Current sensing.

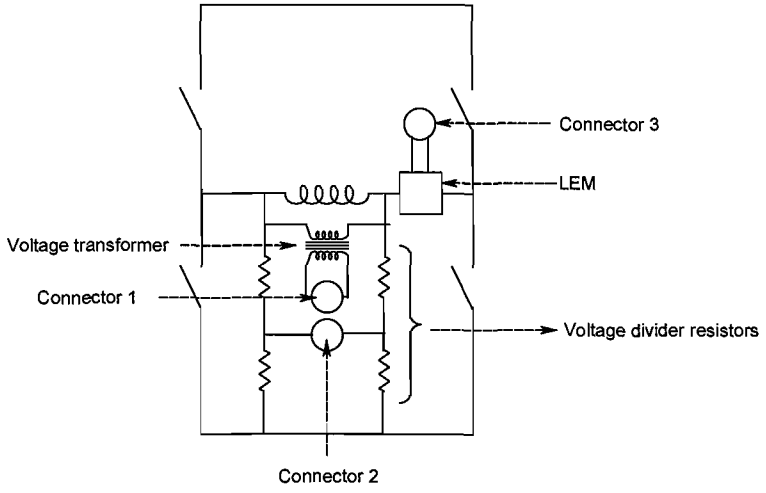

FIGURE 2-6 ADDITIONAL SENSING CIRCUIT ILLUSTRATION

Additional sense circuitry shall be designed in house. Design specifics shall be communicated with Denel via correspondence.

The Additional sense circuitry will perform function F6.6.

2.1.4.5 FUNCTIONAL UNIT 4.5: CURRENT SENSORS

The current sensor shall be used for average current control. The following LEM sensor shall be used: LEM LAH 25-NP. The LEM sensor shall be configured for 3 primary turns.

The current sensors will perform function F6.5

2.1.4.6 FUNCTIONAL UNIT 4.6: HIGH SIDE FLOATING SUPPLY

A high side floating supply shall be implemented to enable 100% duty cycle operation.

2.1.4.7 FUNCTIONAL UNIT 4.7: PROTECTION CIRCUITRY

Protection circuitry shall be implemented to protect the PA from:

1. Over temperature;
2. Over current;
3. Short circuiting (pulse for pulse).

A connection point shall be provided for DC input.

2.2.1.6.1 Electrical/Mechanical interface

Screw terminals.

2.2.1.7 INTERFACE IF7.0: ADDITIONAL INPUT/OUTPUT SIGNALS TO DIGITAL CIRCUITRY

The digital circuitry PCB shall provide an area for easy accessibility of appropriate pins of the embedded devices. These pins will be used for additional input signals.

2.2.1.7.1 Electrical/Mechanical interface

IDC connectors.

2.2.1.8 INTERFACE IF8.0: COMMUNICATION SIGNALS TO DIGITAL CIRCUITRY

Communication interfaces shall be provided to the digital controller.

2.2.1.8.1 Electrical/Mechanical interface

Appropriate connectors that complements the communication line drivers used.

2.2.1.9 INTERFACE IF9.0/10.0: POWER AMPLIFIERS AND ANLOGUE INPUT SIGNALS

The signals from the power amplifiers form part of the analogue input signals. The interface between the analogue input signals and the analogue circuitry is discussed in section 2.2.1.1: IF 1.0.

2.2.1.10 INTERFACE IF11.0: USER INTERFACE WITH INTEGRATED CONTROLLER.

The following interfaces shall be provided to the user:

1. Visual
    a. Power LEDs to indicate if there is power on the circuits;
    b. General purpose LEDs to be assigned by the user;
2. Tactile
    a. Switches for physical interfacing;
3. Programming and debugging
    a. Emulator connection.

2.2.2 ANALOGUE CIRCUITRY INTERFACES

This section's *Electrical/Mechanical* layer interface will be tracks laid out on a PCB

2.2.2.1 INTERFACE IF2.1: BUFFERS, ANTI ALIASING FILTERS AND ADC

No specific requirements

2.2.3 DIGITAL CIRCUITRY INTERFACES

This section's *Electrical/Mechanical* layer interface will be tracks laid out on a PCB

2.2.3.1 INTERFACE IF3.1: EXTERNAL RAM AND EMBEDDED DEVICES

The External RAM shall interface with the DSP via the appropriate port.

2.2.3.2 INTERFACE IF3.2: COMMUNICATION INTERFACE AND EMBEDDED DEVICES.

A high speed communication line driver shall be interfaced with the SPI port of the main embedded device. A low speed communication line driver shall be interfaced with the SCI port of the main embedded device.

2.2.3.3 INTERFACE IF3.3: PWM GENERATION AND EMBDEDDED DEVICES

On chip peripheral PWM generation signals shall be used for PWM generation.

2.2.3.4 INTERFACE IF3.4: I/O EXPANSION AND EMBEDDED DEVICES.

Appropriate pins of the embedded devices shall be made available in the I/O expansion area of the digital circuitry PCB. Detail pin assignment shall be determined via correspondence.

Half of the FPGA device pins that shall be available on the expansion area shall be buffered.

2.2.3.5 INTERFACE IF3.5: JTAG AND EMBEDDED DEVICES

The JTAG port pins of the embedded devices shall interface with the JTAG connector.

2.2.3.6 INTERFACE IF3.6/3.7/3.8: ELECTRONIC SUPPLY INTERFACES WITH OTHER FUNCTIONAL UNITS

Filters shall be implemented between Fly-back Converter and the devices it supplies power to.

2.2.4 POWER AMPLIFIER INTERFACES

2.2.4.1 INTERFACE IF4.1-4.2

No specific requirement

2.2.4.2 INTERFACE IF4.3: 3-PHASE POWER CIRCUIT AND ADDITIONAL SENSE CIRCUITRY.

Interface specifications shall be supplied via correspondence.

2.2.4.3 INTERFACE IF4.4-4.9

No specific requirement

2.2.4.4 INTERFACE IF4.10: PROTECTION CIRCUITRY AND DIGITAL CONTROLLER

The interface between the output of the protection circuitry to the digital circuitry shall be optically isolated.

2.3 SUBSYSTEM FUNCTIONAL CAPABILITY / FLOW

2.3.1 AMB SYSTEM FUNCTIONAL FLOW

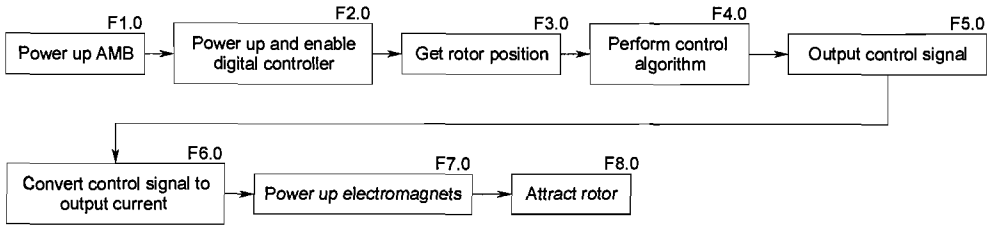

FIGURE 2-7 FUNCTIONAL FLOW OF AMB SYSTEM

2.3.2 USING THE INTEGRATED CONTROLLER: FUNCTIONAL FLOW

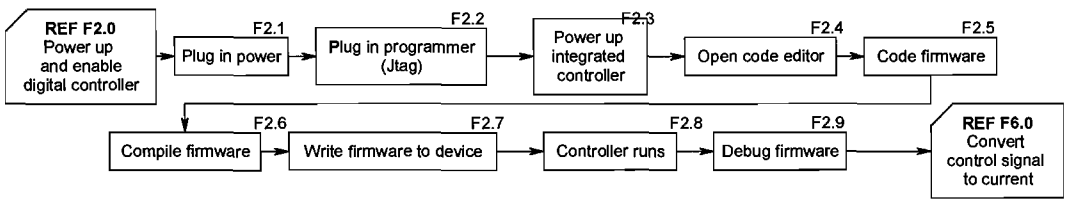

FIGURE 2-8 USING THE INTEGRATED CONTROLLER: FUNCTIONAL FLOW

Fault conditions shall be reported to the main embedded device.

2.1.4.8 FUNCTIONAL UNIT 4.8: FILTERS

Filters should be implemented to remove high frequency components.

2.2 INTERFACES

2.2.1 SYSTEM INTERFACES

2.2.1.1 INTERFACE IF1.0: ANALOGUE INPUT SIGNALS TO ANALOGUE CIRCUITRY

The analogue signals shall be routed to the analogue circuitry through noise immune cabling and connectors.

2.2.1.1.1 Electrical/Mechanical interface

Appropriate:

1. feed through EMI filters;
2. cabling;
3. connectors;

shall be used for the interfacing of the analogue signals to the analogue circuitry.

2.2.1.2 INTERFACE IF2.0: ANALOGUE AND DIGITAL CIRCUITRY

The analogue circuitry shall be "piggy backed on the digital circuitry.

2.2.1.2.1 Electrical/Mechanical interface

Appropriate connectors for interfacing two PCBs.

2.2.1.3 INTERFACE IF3.0: DIGITAL CIRCUITRY TO POWER AMPLIFIERS

The digital circuitry shall be "piggy backed" on the power amplifiers' board. The digital circuitry shall thus be removable from the power amplifiers.

Interface between digital controller and power amplifiers should be optically isolated.

2.2.1.3.1 Electrical/Mechanical interface

Appropriate connectors for interfacing two PCBs.

2.2.1.4 INTERFACE IF4.0: POWER AMPLIFIERS TO ELECTROMAGNETS

No filters shall be implemented on the output of the power amplifiers.

2.2.1.4.1 Electrical/Mechanical interface

1. Shielded twisted pair cabling shall be used for the interface between the power amplifiers and the electromagnets.
2. Screw terminals shall be used for connecting cabling to power amplifiers.

2.2.1.5 INTERFACE IF5.0: JTAG EMULATOR TO DIGITAL CONTROLLER

The digital controller board shall have IEEE 1149.1 JTAG emulation connectors for both embedded devices.

2.2.1.5.1 Electrical/Mechanical interface

14 pin header interfaces.

2.2.1.6 INTERFACE IF6.0: DC SUPPLY TO POWER AMPLIFIERS

2.3.3 FUNCTIONAL CAPABILITIES OF THE CONTROLLER

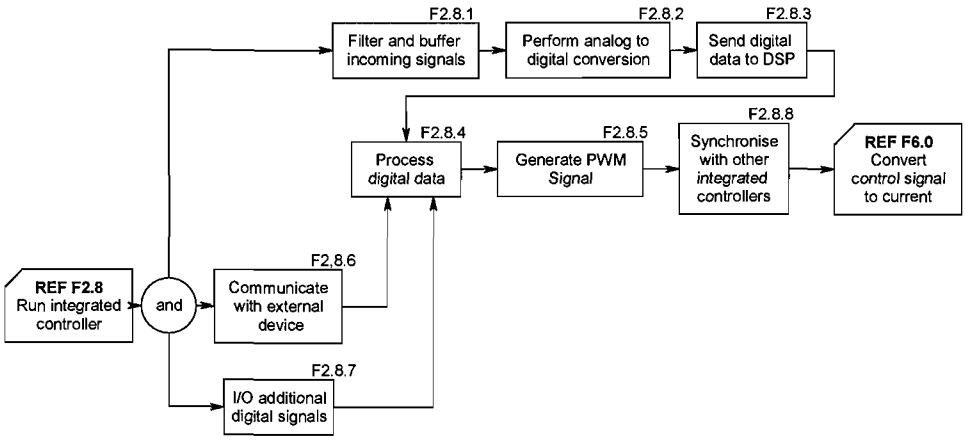

FIGURE 2-9 FUNCTIONS OF THE INTEGRATED CONTROLLER

2.3.3.1 FUNCTION F2.8.1: FILTER AND BUFFER INCOMING SIGNALS

Filters and buffers shall be designed in house. Design specifics shall be supplied to Denel via correspondence.

2.3.3.2 FUNCTION F2.8.2: PERFORM ANALOG TO DIGITAL CONVERSION

The sampling of the ADCs shall be able to synchronize with the PWM signals. Four AD7322 devices shall interface with four dedicated SPI ports on the FPGA.

2.3.3.2.1 Performance requirements

The following table provides the minimum frequency by which the input signals must be sampled. A main embedded device and a co-embedded device shall be implemented. The table illustrates the distribution of the ADCs between the embedded devices.

TABLE 2-2 ADCS ALLOCATION AND REQUIREMENTS

Signal input type	Minimum samples per second	Interface with	Amount of ADCs required	Available for
Position signals	100ksps	Main embedded device	1	External signals
Additional external signals.	100ksps	Main embedded device	3	External signal inputs
Power amplifiers output current	100ksps	Main embedded device	2	PA current sensors
Additional sense signals	1Msps	FPGA	4	PA additional sense circuitry
Additional analogue inputs of main embedded device.	2Msps	Main embedded device	10	I/O expansion area.

1. The sampling of the external ADCs shall be able to synchronize with the generated PWM signals.

2. Two interrupt pins of the co-embedded device shall be available on the analogue circuitry. (interrupt pins shall also be available on the I/O expansion area).

Figure 2-9 illustrates the analogue signals' origin and path to embedded devices.

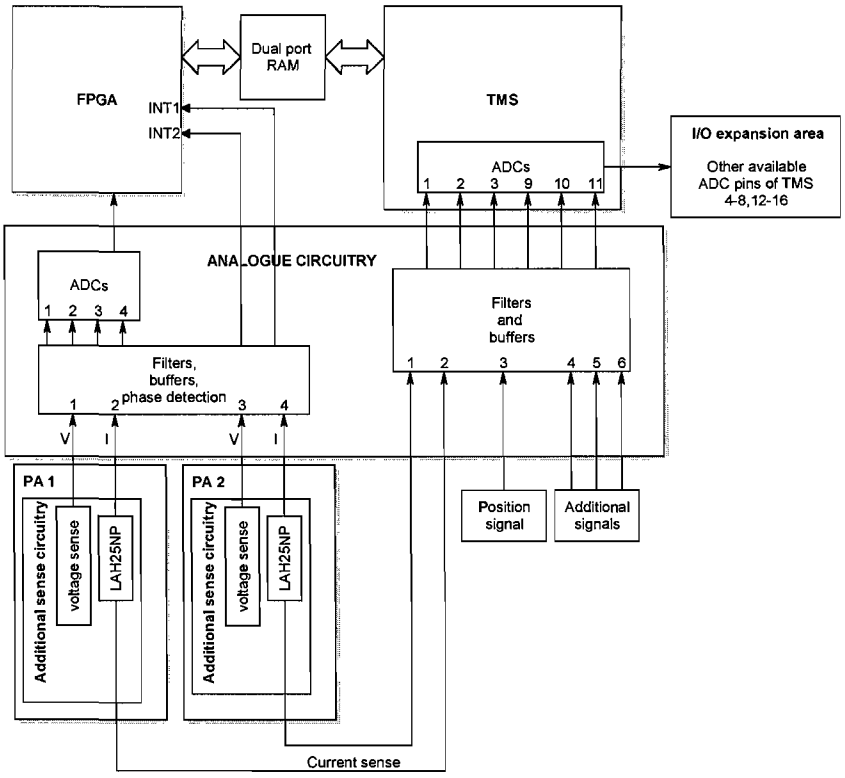

FIGURE 2-10 ANALOGUE INPUT SIGNALS ILLUSTRATION

2.3.3.3 FUNCTION F2.8.3: SEND DIGITAL DATA TO EMBEDDED DEVICE

The digitized signal's data will be sent to the embedded device via the interface between the embedded device and the ADC. External ADCs shall interface with the FPGA through four dedicated SPI ports.

2.3.3.3.1 Performance requirement

External ADCs shall communicate with FPGA at a minimum data of 12Mbps.

2.3.3.4 FUNCTION F2.8.4: PROCESS DATA

The DSP will process the data and generate required outputs by executing firmware.

2.3.3.4.1 Performance requirement

Minimum processing speed of the main embedded device:

150 MIPS

2.3.3.5 FUNCTION F2.8.5: GENERATE PWM SIGNAL

Requirements of the PWM signal are as follows:

2.3.3.5.1 Performance requirement

1. The PWM signal shall have a frequency range of 20 kHz to 50 kHz (Met by internal PWM generator of main embedded device);
2. Shall have a 0-100% variable duty cycle with a resolution of at least 1024 intervals (Met by internal PWM generator of main embedded device);

2.3.3.6 FUNCTION F2.8.6: COMMUNICATE WITH EXTERNAL DEVICE

The DSP shall be able to serially communicate with an external device. One high speed and one low speed communication interface shall be implemented.

2.3.3.6.1 Performance requirement

1. The minimum bit rate of the high speed communication shall be 20Mbps.

   (Worst case: 15 packets per 20KHz cycle. Each packet containing 4x16 bit words.

   15 x 20e3 x 4 x 16 = 19.2 Mbps.)
2. The high speed communication shall use a robust scheme like RS484 or Optical drivers.
3. High speed communication scheme shall support multipoint interfacing. (Main controller to several slave controllers, see Figure 1-1, with half or full duplex communication)
4. Low speed communication shall be implemented on the SCI.
5. Low speed communication shall utilize a RS484 scheme.
6. Low speed communication scheme shall support multipoint interfacing (Main controller to several slave controllers with half or full duplex communication).

2.3.3.7 FUNCTION F2.8.7: INPUT/OUTPUT ADDITIONAL SIGNALS

Generic signals interfacing with the embedded devices.

2.3.3.8 FUNCTION F2.8.8: SYNCHRONISE WITH OTHER INTEGRATED CONTROLLERS

The PWM generator of one integrated controller (for one degree of freedom) should be able to synchronize with the PWM generation of other integrated controllers. This will imply that the controllers will start their PWM time periods on exactly the same instance. This technique significantly reduces noise in an AMB system.

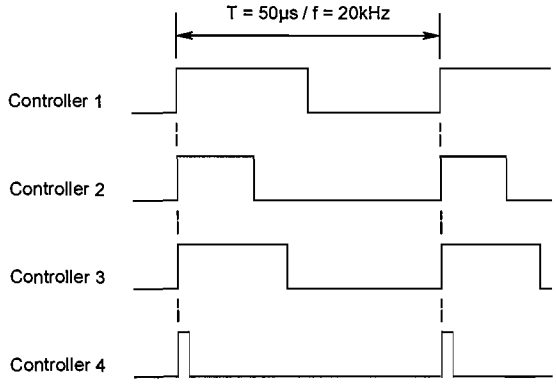

FIGURE 2-11 SINGLE PWM SIGNAL OF FOUR INTEGRATED CONTROLLERS

2.3.3.8.1 Performance requirement

Absolute time delay between start of PWM signals shall not exceed 0.5µs.

2.3.4 FUNCTIONAL CAPABILITIES OF THE POWER AMPLIFIER

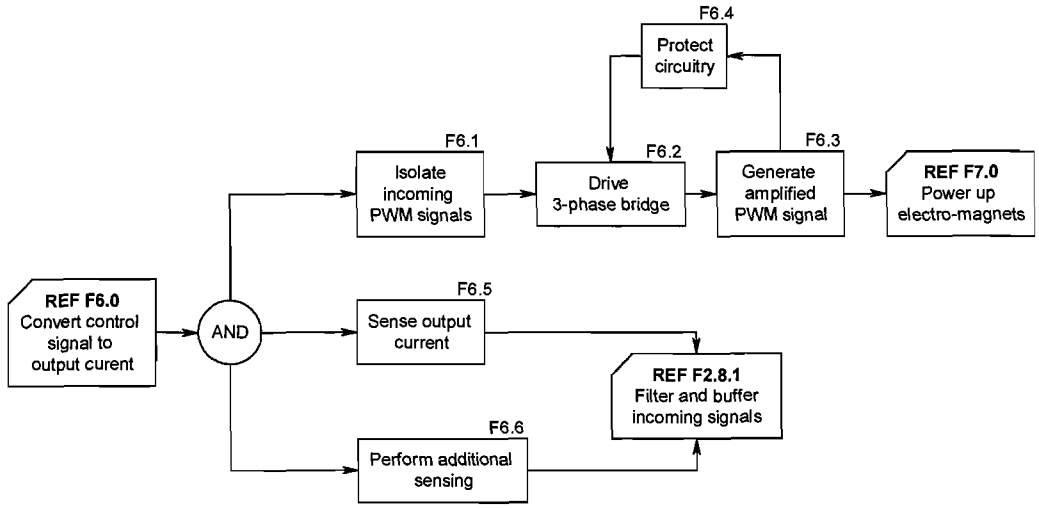

FIGURE 2-12 FUNCTIONS OF THE POWER AMPLIFIER

2.3.4.1 FUNCTION F6.1: ISOLATE INCOMING SIGNALS

The PWM signals generated by the digital circuitry shall be optically isolated from the power amplifiers' circuitry.

2.3.4.1.1 Performance requirement

Opto-coupler bandwidth shall be adequate to transmit PWM signals up to 50kHz.

2.3.4.2 FUNCTION F6.2: DRIVE 3-PHASE BRIDGE

The 3-phase bridge driver shall be selected by the designer.

2.3.4.2.1 Performance requirement

No specific requirement.

2.3.4.3 FUNCTION F6.3: GENERATE AMPLIFIED PWM SIGNALS

The switching devices of the 3-phase bridges shall be forced into an off state under the following conditions:

1. Condition 1
    - Power is still applied to the power amplifiers;
    - The physical connection between the PWM signals from the digital circuitry and power amplifier circuitry has been broken.
2. Condition 2
    - Power is still applied to the power amplifiers;
    - The embedded devices generating PWM signals is not executing any code.

The output of the power amplifiers shall adhere to the following specifications

2.3.4.3.1 Performance requirement

1. Nominal bridge voltage variable between 50 – 150V with 10% tolerance;
2. Nominal output current: 7.5A rms; 15A peak;
3. Switching frequency 20-50kHz.

2.3.4.4 FUNCTION F6.4: PROTECT CIRCUITRY

The power amplifiers shall provide the following protection:

Protection against:

1. Over temperature;
2. Over current;
3. Short circuits.

2.3.4.4.1 Performance requirement

Over temperature: The temperature sensor shall have a sensitivity of approx 2.5 °C.

Over current and short circuit protection: Requirements to be determined by designer of power amplifier.

2.3.4.5 FUNCTION F6.5: SENSE OUTPUT CURRENT

The output current of the PA shall be sensed by a LEM LAH-25NP sensor.

2.3.4.6 FUNCTION F6.6: PERFORM ADDITIONAL SENSING

Additional sensing specifications shall be supplied via correspondence.

2.4 ENVIRONMENTAL REQUIREMENTS

2.4.1 TEMPERATURE

The system shall operate in a normal laboratory environment. Temperature range approx. 0°C – 30°C

2.4.2 HUMIDITY

No specific requirement.

2.4.3 SHOCK AND VIBRATION

No specific requirement.

2.5 DESIGN AND CONSTRUCTION REQUIREMENTS

2.5.1 MATERIALS, PROCESSES, AND PARTS

Materials and components shall be used that are commonly obtainable from secondary suppliers.

2.5.2 MOUNTING AND LABELLING

The integrated controller should be designed to be mountable in a rack. LEDs shall be visible from the front of the rack. Detail specifications shall be communicated via correspondence. Figure 2-12 illustrates the mounting concept.

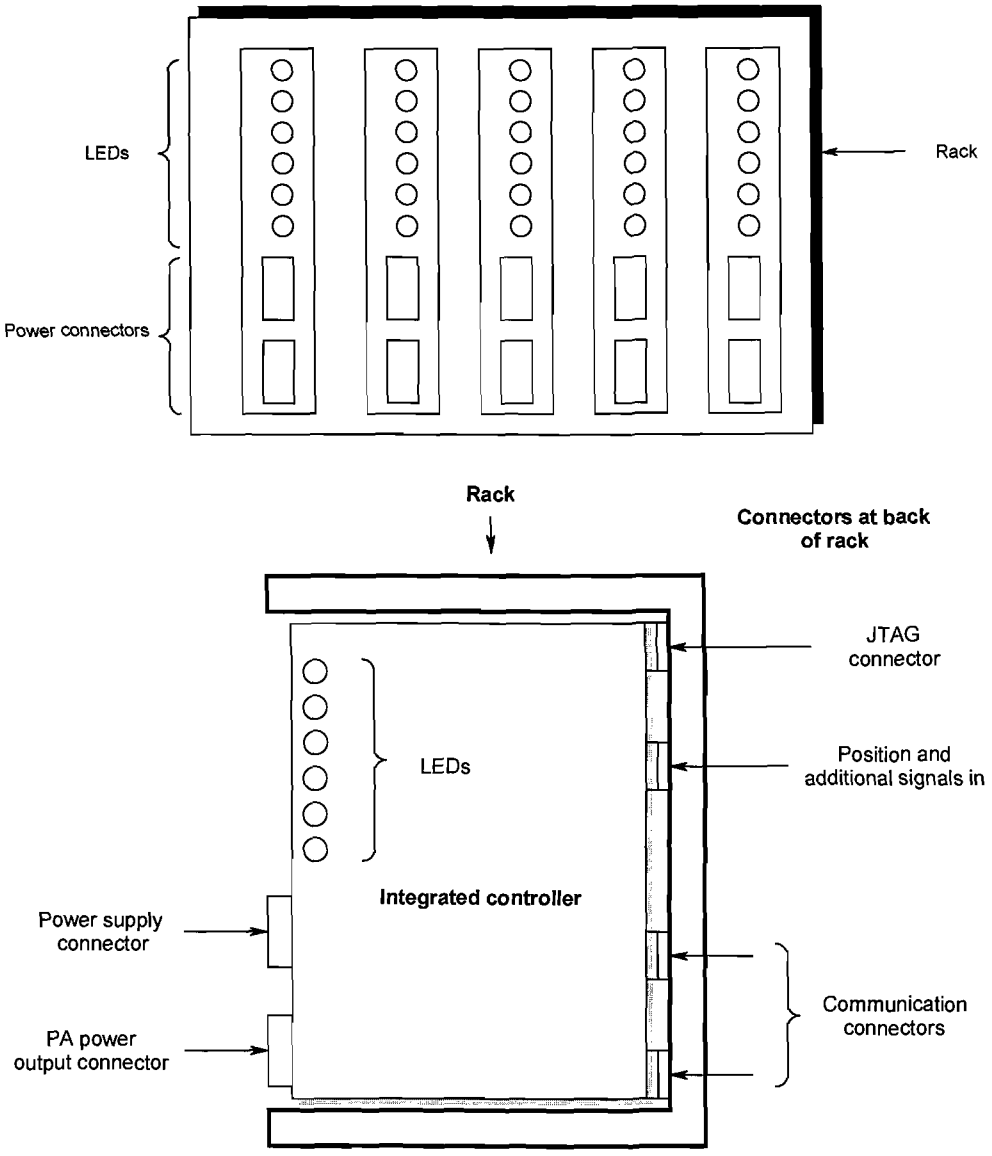

FIGURE 2-13 INTEGRATED CONTROLLER MOUNTING CONCEPT

2.5.2.1 LAYOUT REQUIREMENTS

The Bridge layout of the two power amplifiers shall be symmetrical. Figure 2-13 illustrates the symmetrical concept.

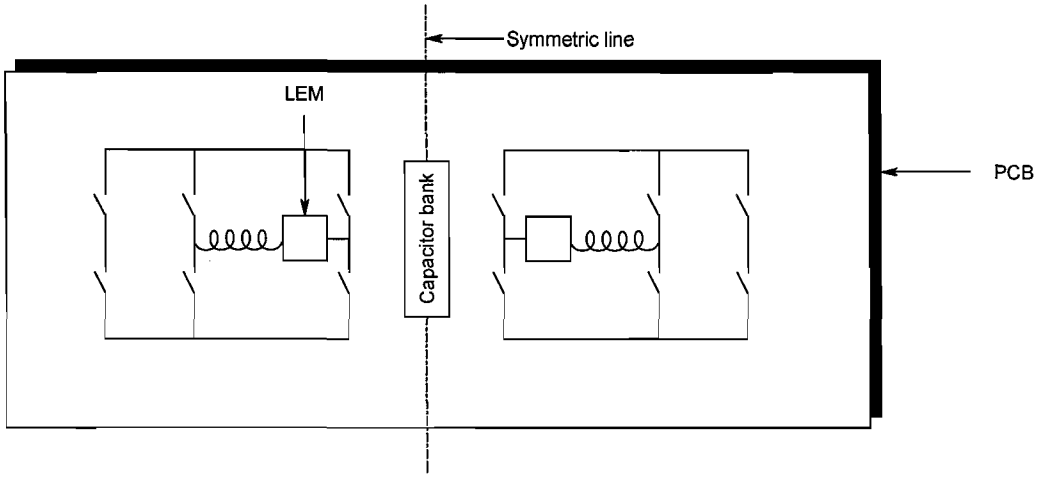

FIGURE 2-14 BRIDGE LAYOUT SYMMETRICAL CONCEPT

2.5.3 ELECTROMAGNETIC RADIATION

The system shall be evaluated according to electromagnetic radiation standards used by Denel.

2.5.4 SAFETY

High voltage and high current carrying conductors shall be isolated to prevent shock from direct touch.

2.5.5 SECURITY

No specific requirement

2.5.6 INTERCHANGE REQUIREMENTS

No specific requirement

2.6 MAINTENANCE AND LOGISTICS

2.6.1 MAINTENANCE CONCEPT AND REQUIREMENTS

2.6.1.1 SCHEDULED MAINTENANCE

No specific requirement

2.6.1.2 UNSCHEDULED MAINTENANCE AND REPAIRS

Maintenance and repairs shall be performed by the MBMC research group at the NWU. If maintenance and repairs requires unavailable skill and equipment, help shall be sought from Denel.

2.6.2 TEST AND SUPPORT EQUIPMENT

Denel shall provide technical reference documentation concerning the integrated controller. Some of the content of the document should include:

1. Interface pin outs;
2. Interface descriptions;
3. Jumper settings description;

4. Test points;
5. Etc.

2.6.3 FIRMWARE UPGRADE SUPPORT

Firmware development, upgrading and testing will be implemented by members of the MBMC research group at the NWU.

2.6.4 PACKAGING, HANDLING, STORAGE, AND TRANSPORTATION

No specific requirement.

3. QUALITY ASSURANCE

3.1 EXAMINATIONS AND TESTS

3.1.1 FACTORY ACCEPTANCE TESTS (FAT)

FATs shall be performed as specified and required by Denel.

3.1.2 SITE ACCEPTANCE TESTS (SAT)

The integrated controller shall be tested in the MBMC lab at the NWU. The integrated controller shall be tested against functionality and performance specifications.

3.1.3 MANUFACTURING QA TESTS

No specific requirements.

3.1.4 TYPE APPROVAL TESTS

No specific requirements.

3.1.5 EXTERNAL QUALIFICATION TESTS / THIRD PARTY TESTS

No specific requirements.

3.1.6 SAFETY TESTS

No specific requirement.

4. APPENDIX A: ACCEPTANCE TEST SHEET

4.1 ACCEPTANCE TEST MATRIX

Requirement	Acceptance requirement					Method and Criteria
	1	2	3	4	5	
Architecture in 2.1	X			X		Refer to method / values
Interfaces in 2.2	X	X		X		Refer to method / values
Functions in 2.3	X	X				Refer to method / values
Environmental in 2.4	X					Refer to method / values
Design in 3.5				X		
Maintenance in 2.6				X		Refer to method / values

4.2 CLASSIFICATION OF ACCEPTANCE METHOD AND CRITERIA

The following acceptance methods shall be applicable:

1. Demonstration: The operation of the system, or a part of the system, that relies on observable *functional* operation not requiring the use of instrumentation, special test equipment, or subsequent analysis.
2. Test: The operation of the system, or a part of the system, using instrumentation or other special test equipment to collect data for later *analysis and reporting.*
3. Analysis: The *processing* of accumulated data obtained from other qualification methods. Examples are reduction, interpolation, or extrapolation of test results.
4. Inspection: The *visual* examination of system components, documentation, etc.
5. Special qualification methods. Any special *qualification* methods for the system, such as special tools, techniques, procedures, facilities, acceptance limits, use of standard samples, pre-production or periodic production samples, pilot models, or pilot lots.

The following sub-categories may be applicable:

A. Computer software test

B. Internal qualification test (at factory, not acceptance test)

C. External qualification test (at independent third party, not acceptance test)

CONFIGURATION CONTROL

DOCUMENT HISTORY

Issue	Date	Status	Editor	Filename on disk
02A	2006-05-23	Draft	MSWord	
02B	2006-06-19	Semi final		
02C	2006-08-08	Semi Final		

REVISION HISTORY

Issue	Date	Changes
01A	2006-04-26	First draft
02A	2006-05-23	All architectures, functions and contents updated.
02B	2006-06-19	"To be discussed" items in previous issue have been updated.
02C	2006-08-08	Updated items: ADC, Additional sensing, PA spec, mechanical layout, analogue circuitry, Current sensor

Appendix B: Data CD

Table of content:

- Documentation
- Measurements
- Photos

Firmware, schematics and layouts are not included on the data CD due to intellectual property reasons.