

Chapter 3

Conceptual design of the total communication system

This chapter will present the conceptual design of the total communication system including the internal communication and the external communication. A design process will be described and put into practice to select the optimum solution for each of the specified interfaces. Lastly the chapter will conclude with a clear motivation of each of the final selections.

3.1 Introduction

After a comprehensive literature study was conducted the conceptual design commences. The conceptual design will include the following:

1. A short description of the ADES requirements.
2. Formulation of the different architecture options for the ADES.
3. Selection of the appropriate architecture for the ADES.
4. Development of a design process to design the internal and external communication systems for the ADES.
5. Selection of the optimum solution for each of the interfaces.
6. Final evaluation of the communication system.

3.2 ADES requirements overview

A detailed description of the functionality of the ADES was given in chapter 1. All the requirements and specifications of the system were thoroughly documented in the "Systems requirements specification for the AMB - and drive electronic system (ADES)" [46]. This document was generated to aid in the development of the different functional units of the system. In this

specific section only a short overview of the document will be given. For more information refer to Appendix B.1.

Figure 3-1 shows the various interfacing entities of the ADES – indicated by IF x.0. In the “Systems requirement specification for the ADES”, only the external interfacing entities were listed and specified. The interface label IF 1.0 was reserved to be used by the designer of the communication sub-system to specify all the necessary internal interfaces.

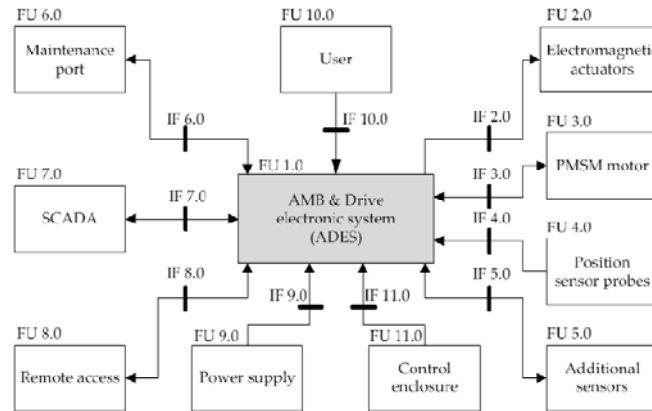


Figure 3-1: Interfacing entities of the ADES.

It must be noted that not all the indicated interfacing entities are of importance for the development and design of the communication sub-system of the ADES. The specified external interfacing entities that will be focussed on are:

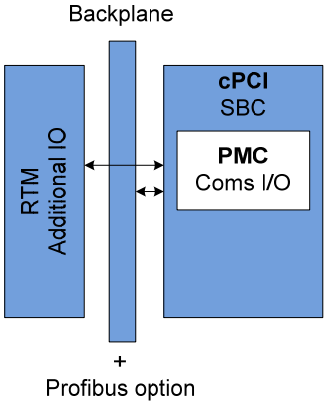
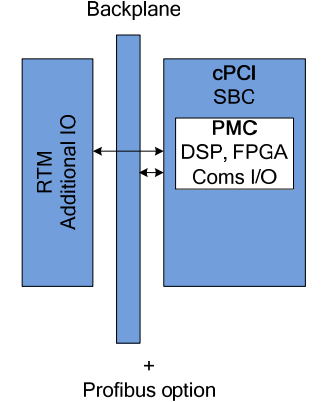
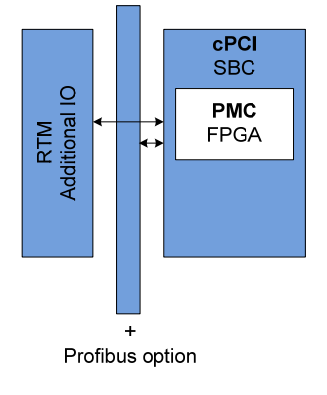
- Maintenance port (FU 6.0)
- SCADA (FU 7.0)
- Remote access (FU 8.0)

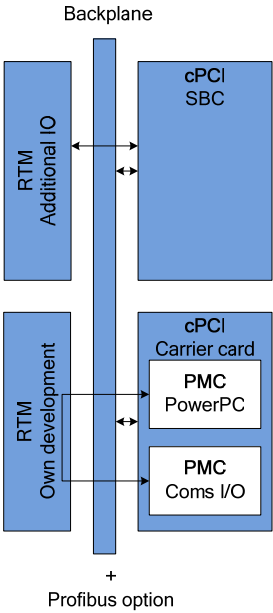
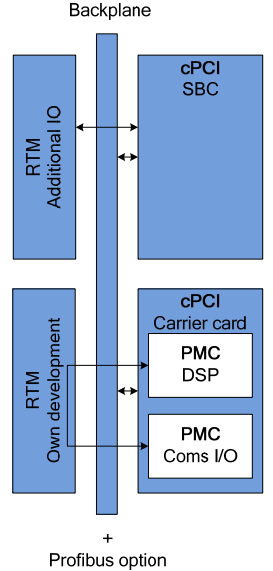
For more information on the requirements and specifications of these three external interfacing entities refer to Appendix B.1. Besides from focussing on specifying the appropriate protocol for these three interfaces, the main focus will also be on designing and a developing internal communication system for the ADES. At this stage the internal interfaces cannot be identified, this will be done after the final architectural concept of the ADES are described and explained.

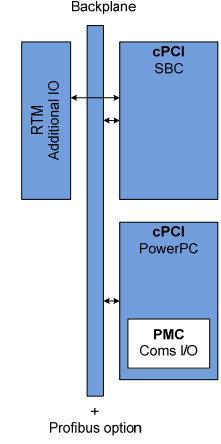
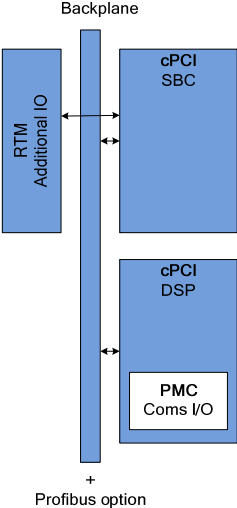
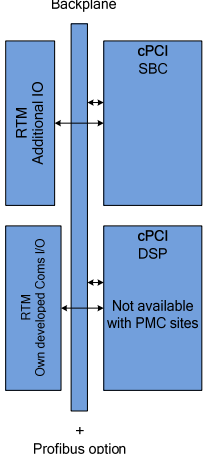
3.3 ADES architecture options

Before commencing to the communication sub-system design and development, it is necessary to select the appropriate system architecture. In this section various ADES architecture options will be formulated, the pros and cons will be listed and the best architecture will be selected. This part of the conceptual design will be of utmost importance, bearing in mind that this will have an influence on the design and development of the communication sub-system for the ADES.

Table 3-1: Architecture description

Option	Functionality	Architecture illustration
1	<ol style="list-style-type: none"> 1. All the control algorithms, user interfaces, system monitoring functions and data logging functions as stipulated in the "Systems requirement specifications document" will be done on a Single Board Computer (SBC). The SBC will be a CompactPCI system. 2. The communication to the various functional units will be done by a selected Peripheral Component Interconnect Mezzanine Card (PMC) and placing it one of the SBC's PMC sites. 3. The system will also allow additional interfaces to some of the functional units via a Rear Transition Module (RTM). This functionality will be the same for all the options. 4. The Profibus options will be discussed in Section 3.14.3 at this stage it is only necessary to know that a Programmable Logic controller (PLC) will interface with the main controller by means of a selected Profibus card. This function will also be the same for all the options. 5. All the selected cards will adhere to the PCI standard. 	 <p>The diagram for Architecture 1 shows a vertical Backplane connecting three main components. On the left is a vertical bar labeled 'RTM Additional IO'. On the right is a larger vertical bar labeled 'cPCI SBC'. Inside the 'cPCI SBC' bar is a smaller box labeled 'PMC Coms I/O'. Bidirectional arrows connect the 'RTM Additional IO' bar to the 'Backplane', and the 'Backplane' to the 'cPCI SBC' bar. Below the 'Backplane' label is a '+' sign and the text 'Profibus option'.</p> <p>Figure 3-2: Architecture 1</p>
2	<ol style="list-style-type: none"> 1. In this architecture the SBC will only be used for monitoring, data logging and user interfaces. 2. The control algorithms will run on a Digital Signal Processor (DSP) situated on the PMC and the communication to the various functional units will be done on an FPGA situated on the same PMC card. 	 <p>The diagram for Architecture 2 shows a vertical Backplane connecting three main components. On the left is a vertical bar labeled 'RTM Additional IO'. On the right is a larger vertical bar labeled 'cPCI SBC'. Inside the 'cPCI SBC' bar is a smaller box labeled 'PMC DSP, FPGA Coms I/O'. Bidirectional arrows connect the 'RTM Additional IO' bar to the 'Backplane', and the 'Backplane' to the 'cPCI SBC' bar. Below the 'Backplane' label is a '+' sign and the text 'Profibus option'.</p> <p>Figure 3-3: Architecture 2</p>
3	<ol style="list-style-type: none"> 1. The SBC will be used for the same functions as specified in option 2. 2. In this architecture both the control algorithms and the communication will run on an FPGA situated on the same PMC. This particular FPGA will include an embedded Performance Optimized with Enhanced RISC Processor Chip (PowerPC) which will be used to execute the control algorithms. 	 <p>The diagram for Architecture 3 shows a vertical Backplane connecting three main components. On the left is a vertical bar labeled 'RTM Additional IO'. On the right is a larger vertical bar labeled 'cPCI SBC'. Inside the 'cPCI SBC' bar is a smaller box labeled 'PMC FPGA'. Bidirectional arrows connect the 'RTM Additional IO' bar to the 'Backplane', and the 'Backplane' to the 'cPCI SBC' bar. Below the 'Backplane' label is a '+' sign and the text 'Profibus option'.</p>

		<p>Figure 3-4: Architecture 3</p>
4	<ol style="list-style-type: none"> 1. The SBC will be used for the same functions as specified in option 2. 2. The control algorithms execute on a PMC which consists of a PowerPC. The communication between the various functional units will be handled by another PMC. Both of these PMCs will slot into PMC sites situated on a CompactPCI carrier card. 3. This architecture will require the development of an RTM which routes the signal from the PMC consisting of the PowerPC to the PMC card which handles the communication I/O. This must be done to avoid the use of the PCI bus in real time scheduling. 	 <p>The diagram shows a vertical Backplane. On the left, there are two blue boxes: 'RTM Additional IO' and 'RTM Own development'. On the right, there are two blue boxes: 'cPCI SBC' and 'cPCI Carrier card'. The 'cPCI Carrier card' contains two white boxes: 'PMC PowerPC' and 'PMC Coms I/O'. Bidirectional arrows connect 'RTM Additional IO' to the Backplane, and 'RTM Own development' to the Backplane. Bidirectional arrows also connect the Backplane to 'cPCI SBC' and 'cPCI Carrier card'. Below the diagram is a plus sign and the text 'Profibus option'.</p> <p>Figure 3-5: Architecture 4</p>
5	<ol style="list-style-type: none"> 1. This architecture is almost similar to the previously mentioned architecture; the only difference is that the PMC consisting of a PowerPC will now be replaced by a PMC consisting of a DSP. All the other system architecture attributes remain the same. 	 <p>The diagram is similar to Figure 3-5, showing a vertical Backplane. On the left, there are two blue boxes: 'RTM Additional IO' and 'RTM Own development'. On the right, there are two blue boxes: 'cPCI SBC' and 'cPCI Carrier card'. The 'cPCI Carrier card' contains two white boxes: 'PMC DSP' and 'PMC Coms I/O'. Bidirectional arrows connect 'RTM Additional IO' to the Backplane, and 'RTM Own development' to the Backplane. Bidirectional arrows also connect the Backplane to 'cPCI SBC' and 'cPCI Carrier card'. Below the diagram is a plus sign and the text 'Profibus option'.</p> <p>Figure 3-6: Architecture 5</p>

6	<ol style="list-style-type: none"> 1. The SBC will be used for the same functions as specified in option 2. 2. The control algorithm will execute on a cPCI card consisting of a PowerPC. 3. The communication to the various functional units will be done by a selected PMC which in this architecture will slot into one of the PowerPC's PMC sites. 	 <p style="text-align: center;">Figure 3-7: Architecture 6</p>
7	<ol style="list-style-type: none"> 1. This architecture is almost similar to the previously mentioned architecture; the only difference is that the CompactPCI card consisting of a PowerPC will now be replaced by a CompactPCI consisting of a DSP. All the other system architecture attributes remain the same. 	 <p style="text-align: center;">Figure 3-8: Architecture 7</p>
8	<ol style="list-style-type: none"> 1. The SBC will be used for the same functions as specified in option 2. 2. The control algorithms will be done by a CompactPCI DSP card which does not have any PCI slots located on the CompactPCI card. 3. The communication will be done by developing a RTM card which can interface directly with the CompactPCI DSP card. The RTM will consist of communication drivers and an FPGA. 	 <p style="text-align: center;">Figure 3-9: Architecture 8</p>

3.3.1 Pros vs. Cons

Table 3-2: Pros and cons of different architectures

Option	Pros	Cons
1	<ol style="list-style-type: none"> 1. This option requires fewer cards, resulting in a cheaper solution. 2. Fewer cards are used, thus system integration is also simplified. 	<ol style="list-style-type: none"> 1. This option will require real time operating system programming skills which will require a steep learning curve. Possibly delaying the project delivery time.
2	<ol style="list-style-type: none"> 1. This option will also require fewer cards, resulting in a cheaper solution. 2. Fewer cards are used, thus system integration will also be simplified. 	<ol style="list-style-type: none"> 1. A PMC card that consists of a DSP, FPGA and communication drivers was not found. 2. This option will require VHDL programming skills.
3	<ol style="list-style-type: none"> 1. This option will also require fewer cards, resulting in a cheaper solution. 2. Fewer cards are used, thus system integration will also be simplified. 3. FPGAs are very powerful processors which can do parallel processing. 	<ol style="list-style-type: none"> 1. This option will require VHDL programming skills.
4	<ol style="list-style-type: none"> 1. By using this architecture rapid prototyping will be possible, because the programming skills required are less advanced. (For example no real time operating system is required Windows can be used on the SBC and no VHDL programming skills are required) 2. There are multiple manufacturers for these cards. 	<ol style="list-style-type: none"> 1. This option will be far more expensive. 2. A custom RTM needs to be developed.
5	<ol style="list-style-type: none"> 1. Rapid prototyping will again be possible, because the skills required are less advanced. 2. There are multiple manufacturers for these cards. 	<ol style="list-style-type: none"> 1. This option will be far more expensive. 2. A custom RTM needs to be developed.
6	<ol style="list-style-type: none"> 1. Rapid prototyping will again be possible, because the skills required are less advanced. 	<ol style="list-style-type: none"> 1. This option will be far more expensive because PowerPC CompactPCI cards are very expensive.
7	<ol style="list-style-type: none"> 1. By using this architecture it will be possible to do rapid prototyping, because the programming skills required are less advanced. 	<ol style="list-style-type: none"> 1. This option will be far more expensive keeping in mind that a DSP CompactPCI card is very expensive. 2. Cards found had multiple DSPs increasing implementation complexity. 3. These cards only have one manufacturer.
8	<ol style="list-style-type: none"> 1. The programming skills required are less advanced. 	<ol style="list-style-type: none"> 1. This option will require the development of a custom RTM. 2. Integration will take longer. 2. This option will be very expensive.

3.3.2 Final architecture selection

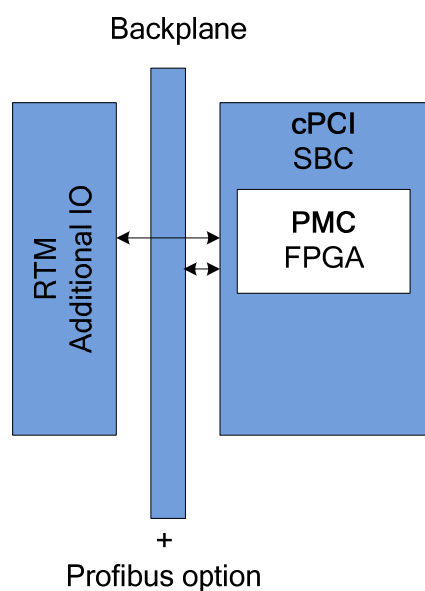
When it came to the final architecture selection the deciding factors were (in order of importance) as found in Table 3-3.

Table 3-3: Deciding factors of architecture selection

Deciding factors	Description
Cost	The cost of the total system may not exceed R150 000.
Processor power	The ability to do floating point operations as well as be able to do parallel (concurrent) processing.
Flexibility &Expandability	The ability to improve the system without changing the system radically.
Future development	The possibility of developing the required cards in the future.

System three as illustrated in Figure 3-10 was the only system that met all these requirements.

1. It was by far the most cost effective system.
2. FPGAs are the most powerful processor with the ability to process commands concurrently.
3. The system did not need any alterations to add new features, making the system expandable and flexible.
4. Only one PMC card was required, thus developing this card in the future would be possible.

**Figure 3-10: Selected system architecture.**

3.4 Communication system requirements

After selecting the best suited system architecture the design and development of the communication sub-system for the ADES can commence. The “Systems requirement specification for the ADES” only stipulates the requirements of the external communication interfaces. The internal communication interface requirements will be discussed in Section 3.8.1, Section 3.9.1, Section 3.10.1 and Section 3.12.1 of this chapter and the external communication interface requirements will be discussed in Section 3.14.1, Section 3.14.2 and Section 3.14.3 of this chapter.

3.5 Design process

Before commencing with the conceptual design of both the internal communication interfaces and the external communication interfaces a design process must be formulated. The design process will entail identifying communication interfaces and conducting detailed trade-off studies to select from two or more options the optimum communication solution for each interface. A trade-off study forms a part of a larger system engineering process [47].

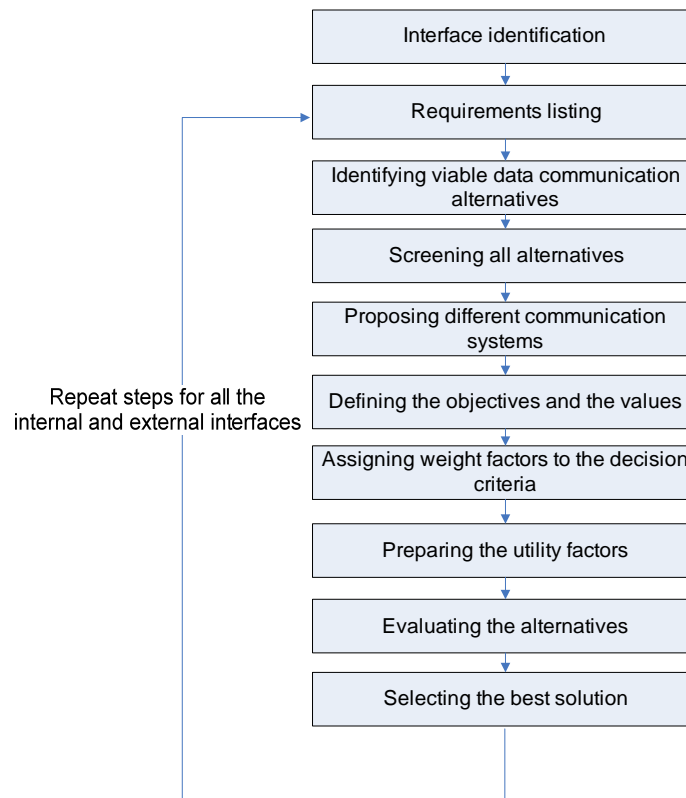


Figure 3-11: Design process [47]

This particular formal trade-off study will be thoroughly documented, where after the preferred architecture will be selected. Considering that the design process entails a detailed trade-off study, the design process will consist of all the necessary steps that the trade-off study will follow as illustrated in Figure 3-11.

3.6 Internal interface identification

Figure 3-12 displays the internal ADES interfacing entities which are indicated by IF 1.x.

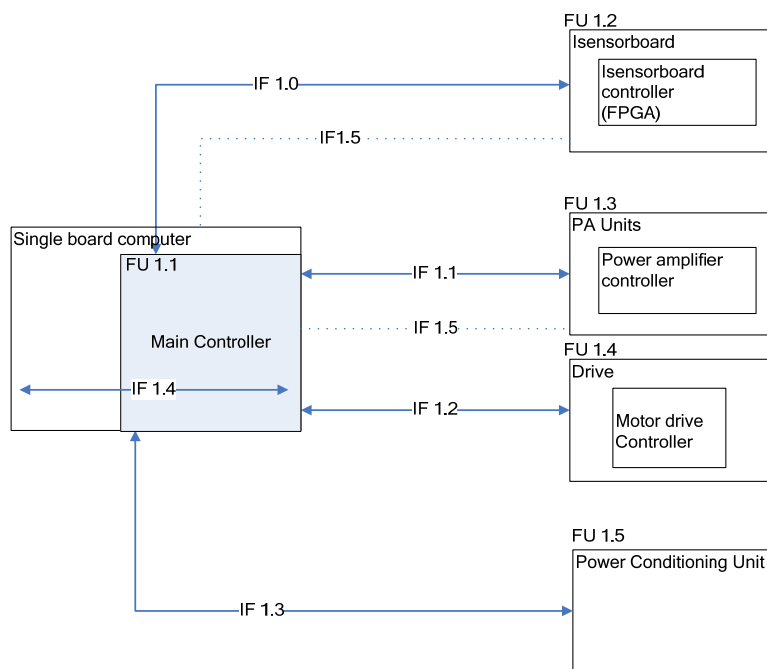


Figure 3-12: Internal interface identification

3.7 Engineering trade-off study

The engineering trade-off study method provides a structured, analytical framework for evaluating alternative architectures. When the engineering trade-off study method is followed to aid in selecting the preferred architecture, the process assumes that the functions and requirements are go/no-go constraints. To qualify as an alternative, architectures must perform all of the identified functions and meet all the identified requirements. The engineering trade-off study method will be followed for each of the internal and external interfaces, to aid in designing the optimum communication sub-system for the ADES.

3.8 Trade-off study for IF1.1

The first trade-off study will determine the optimum data communication standard that will be implemented between the main controller (FU 1.1) and the five power amplifier boards (FU 1.3). Each of the power amplifier boards will consist of two power amplifiers.

3.8.1 Requirements

In this section the requirements will be listed for IF1.1. These requirements will be considered to be go/no-go constraints. If a communication method does not meet these requirements, it cannot be listed as a viable alternative.

3.8.1.1 Constraint 1

Requirement: Minimum data refresh rate (<i>clock frequency</i>)	20 kHz
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The implication of this requirement is that a high data transfer rate will be required, thus it will be necessary to determine the data transfer rate. The minimum data transfer rate will be considered as a constraint. If this constraint is not met by the listed communication methods, it will not be selected as a viable alternative.

3.8.1.2 Minimum data transfer rate

The amount of data that a system can transfer at a time is normally defined either in bits per second (bps) or bytes per second (B/s). The more bits that must be transferred, the faster the data transfer rate must be. For serial busses the data transfer rate will be defined in bps, and for a parallel bus the data transfer rate will be defined in B/s [4]. The transfer of data occurs in regular intervals, which is defined by the period of the transfer clock, here after referred to as the clock time interval. This specific period can be defined as a time interval (in seconds) or as a frequency (in hertz). If the specified clock frequency is 20 kHz then the clock time interval in seconds can be calculated by using (3.1).

$$\begin{aligned}
 \text{Clock interval} &= \frac{1}{f} \\
 &= \frac{1}{20 \times 10^3} \\
 &= 50 \mu\text{s}
 \end{aligned} \tag{3.1}$$

Data transfer rate (bps) can be expressed by (3.2) or (3.3) [5].

$$\text{data transfer rate} = \frac{\text{Number of bits transmitted per operation [bits]}}{\text{Transfer time per operation [seconds]}} \quad (3.2)$$

$$\text{data transfer rate} = [\text{Number of bits transmitted per operation} \times \text{clock interval}] \quad (3.3)$$

The data that must be communicated between the main controller and power amplifiers are listed in Table 3-4.

Table 3-4: Refined functional analysis

Functional Unit	Internal communication			Functional Unit
FU 1.1 Main controller				
	F1.4 Communicate			
		F1.4.1 Transmit		
			F1.4.1.18 Tx: current reference	FU1.3 Power amplifiers
		F1.4.2 Receive		
			F1.4.2.9 Rx: current values	FU1.3 Power amplifiers
			F1.4.2.10 Status	FU1.3 Power amplifiers

By using Table 3-4 the number of bits that must be transmitted per clock time interval between the power amplifiers and the main controller can be calculated as shown in Table 3-5.

Table 3-5: Amount of data to be communicated

Functional Unit	Internal communication			Functional Unit	Bits
FU1.1 Main controller					
	F1.4 Communicate				
		F1.4.1 Transmit			
			Status	FU1.3 Power amplifiers	16
			Current reference	FU1.3 Power amplifiers	16
			Error checking	FU1.3 Power amplifiers	16

		F1.4.2 Receive			
			Current values	FU1.3 Power amplifiers	32
			Status	FU1.3 Power amplifiers	16
			Error checking	FU1.3 Power amplifiers	16
				Total bits per power amplifier	112
				Total bits for 5 power amplifiers with	560

The data transfer rate² can now be calculated by using (3.3)

$$\begin{aligned} \text{Data transfer (bps)} &= 560[\text{bits}] \times 20 \times 10^3 [\text{Hz}] \\ &= 11.2 \text{ Mbps} \end{aligned} \quad (3.4)$$

3.8.1.3 Constraint 2

Requirement: Communication link distance	2 m
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The implication of this requirement is that the selected communication method must be able to transmit the data signal over 2 m without disintegration of the signal. This requirement will directly be considered as a constraint. If this constraint is not met by the listed communication methods, it will not be selected as a viable alternative.

3.8.1.4 Constraint 3

Requirement: Maximum number of slaves	5
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Requirement: Maximum number of masters	1
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Requirement: Communication direction	Bi-directional
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These requirements will be directly considered as a constraint, if these constraints are not met by the listed communication methods it will not be selected as a viable alternative.

² The data transfer rate does not include overhead.

3.8.2 Identify viable data communication alternatives

Various communication methods are listed in Table 3-6. These communication methods will be narrowed down by selecting only the communication methods that adhere to the go/no go constraints. It must be noted that not all the data transmission standards listed in Table 3-6 are full interface standards. Some only specify the physical layer for example RS 485 while others for example the USB data transmission standard specifies the full interface including the protocol (All this information was thoroughly documented in Chapter 2). However all these communication methods are still classified as data transmission standards and will be compared in such a way that detail of each of the data transmission standards are still considered. The remaining viable data transmission standards are listed in Table 3-10.

Table 3-6: Data transmission standards

1.	RS 485	11.	PCI
2.	RS 232	12.	GPIB
3.	I2C	13.	1- Wire
4.	SPI	14.	SMBUS
5.	Microwire	15.	MBUS
6.	USB1 & USB2	17.	LIN Bus
7.	CAN bus	18.	IEEE 1284
8.	TIA/EIA 899	19.	Fibre optic communication
9.	TIA/EIA 644		
20.	RS 422		

3.8.2.1 Screening 1

During the first screening, the following data transmission standards were eliminated due to inability to reach the high data transfer rate required.

Table 3-7: Screening 1

1.	RS 232
2.	I2C
3.	USB1
4.	CAN bus
5.	1-Wire

6.	SMBUS
7.	LIN Bus
8.	Microwire

3.8.2.2 *Screening 2*

During the second screening the following data transmission standards were eliminated due to the inability to communicate over the required distance.

Table 3-8: Screening 2

1.	SPI
2.	PCI

3.8.2.3 *Screening 3*

During the third screening the following data transmission standards were eliminated due to the inability to communicate in both directions.

Table 3-9: Screening 3

1.	RS 422
2.	TIA/EIA 644

3.8.2.4 *Viable communication alternatives*

The remaining alternatives that satisfy the constraints are shown in Table 3-10.

Table 3-10: Viable communication alternatives

1	RS 485
2	TIA/EIA 899
3	USB 1 & USB2
4	IEEE 1284
5	Fibre optic communication

The data transmission standards listed in Table 3-10 will now be used to construct various communication systems between the power amplifiers and the main controller. These different systems will then be evaluated thoroughly.

3.8.3 Proposed communication systems

3.8.3.1 System 1

Communication system 1 proposes to use the data transmission standard RS 485. The main specifications of RS 485 are summarized in Table 3-11.

Table 3-11: RS 485 specifications

Mode of operation	Allowed transmit and receive nodes	Maximum cable length	Maximum data transfer rate
Multipoint, Differential signalling	TX: 32 RX: 32	1200 m	35 Mbps

This proposed architecture is illustrated in Figure 3-13. The data transmission standard employs the simple daisy chaining interconnection method, where device A is connected to device B and device B is connected to device C and the last device is wired to a terminator.

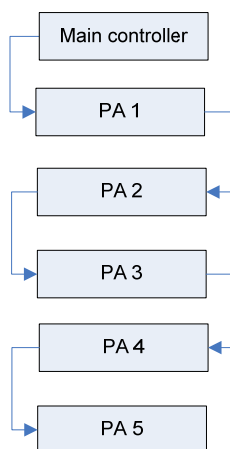


Figure 3-13: Proposed communication system 1

This particular architecture satisfies all the constraints.

3.8.3.2 System 2

Another proposed communication system which will implement the same data transmission standard is illustrated in Figure 3-14. The only difference between the proposed communication system 2 and the proposed communication system 1 is in this case a point-to-point structure will be implemented where all the nodes has an individual communication channel connecting the main controller and the power amplifiers.

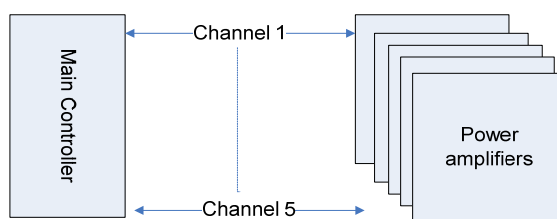


Figure 3-14: Proposed communication system 2

3.8.3.3 System 3

Communication system 3 proposes to use the data transmission standard TIA/EIA 899. The main specifications of the TIA/EIA 899 standard are summarized in Table 3-12.

Table 3-12: TIA/EIA 899 specifications [14]

Mode of operation	Allowed transmit and receive nodes	Maximum cable length	Maximum data transfer rate
Multipoint	32	30 m	500 Mbps

The proposed architecture is exactly the same as the architecture illustrated in Figure 3-13. The only difference between these standards is the maximum data transfer rate, due to low voltage differential signalling. This particular architecture satisfies all the constraints.

3.8.3.4 System 4

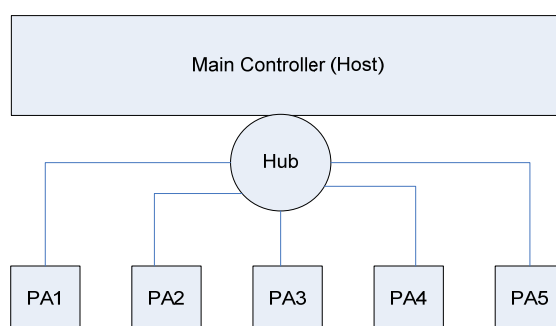
Communication system 4 proposes to use USB 2. The specifications of USB 2 are summarized in Table 3-13. It must be noted that this is a full interface standard³.

³ A full interface standard not only specifies the electrical layer, but also an advanced protocol.

Table 3-13: USB2 specifications [14]

Mode of operation	Allowed transmit and receive nodes	Maximum cable length	Maximum data transfer rate
Multipoint	127	5 m	480 ⁴ Mbps

The proposed architecture is illustrated in Figure 3-15. This specific architecture is realized by connecting a hub to the main controller and connecting each of the power amplifiers to the hub. This can also be referred to as a star interconnection method [14]. This particular architecture satisfies all the constraints.

**Figure 3-15: Proposed communication system 4**

3.8.3.5 System 5

Communication system 5 proposes to use a parallel communication technique to communicate between the power amplifiers and the main controller. Although the majority of the parallel communication techniques are not able to attain constraint 2 (the required distance), the IEEE 1284 standard is able to achieve this constraint [14]. The specifications are shown in Table 3-14 and the proposed architecture as shown in Figure 3-16.

Table 3-14: IEEE 1284 specifications [14]

Mode of operation	Allowed transmit and receive nodes	Maximum cable length	Maximum data transfer rate
Multipoint	8	10 m	16 channels, 64 Mbps @4 MHz clock

⁴ This is the theoretical maximum and a great deal of the frames is overhead.

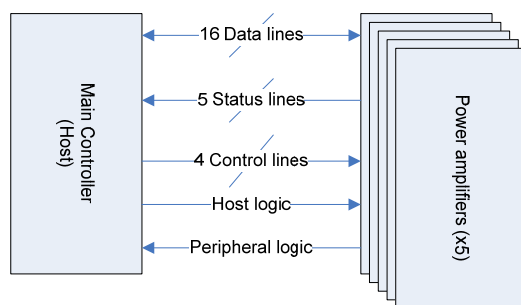


Figure 3-16: Proposed communication system 5

3.8.3.6 System 6

Communication system 6 proposes to use a fibre optic communication method between the power amplifiers and the main controller. The specifications of fibre optic communication are given in Table 3-15. Once again this interface standard only specifies the physical layer.

Table 3-15: Fibre optic specifications

Mode of operation	Allowed transmit and receive nodes	Maximum cable length	Maximum data transfer rate
Point-to-point	1	100 km	>50 Mbps
Star			
Ring			
Logical bus			

One of the proposed communication systems is shown in Figure 3-17. In this case a point-to-point structure will be implemented where each of the nodes has an individual transmit and receive fibre (full duplex) connected directly from the main controller to the power amplifiers. This particular architecture satisfies all the listed constraints.

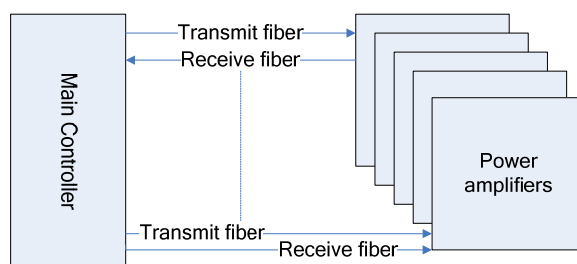


Figure 3-17: Proposed communication system 6

The next proposed communication system will also implement fibre optics. As illustrated in Figure 3-18 a logical bus structure will be implemented where all the nodes are connected by one

common line. This means when one node transmits data all the nodes will receive the data nearly simultaneously, but only the addressed node will respond. This architecture satisfies all the constraints.

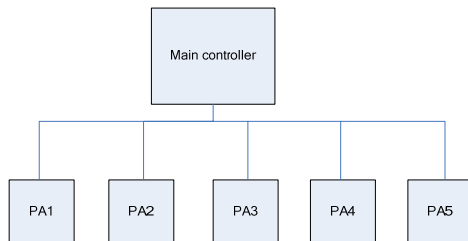


Figure 3-18: Proposed communication system 7

3.8.4 Define objectives and values

Defining the objectives and the values is necessary to once again summarize the important requirements that need to be attained for each interface.

- To ensure effective bi-directional communication between the main controller and the power amplifier units over a maximum distance of 2 m.
- To communicate the correct data between the power amplifiers and the main controllers.
- To refresh all the values every 50 μ s.
- To receive the status of the power amplifiers continuously.
- To implement a method of error detection.

3.8.5 Decision criteria

In order to evaluate the different alternatives and select the optimum communication system a decision criteria is necessary. The main goal of establishing a decision criterion is to list the most important factors which will influence the selection and give a short description of each of the factors.

Table 3-16: Decision Criteria

Decision criteria	Criteria description
Robustness	Noise immunity of the data transmission standard.
Efficiency	Level of error detection and correction implemented in the data transmission standard.
Cost	Cost of implementing the selected data transmission standard.
Risk	Technical implementation risk.
Reliability	The reliability of various components used to implement the data transmission

	standard.
Flexibility & Expandability	The ability to expand the system, for example to increase the data transfer rate to enable the transmission of more data per time interval.

3.8.6 Assign weight factors

The weight factors should be assigned according to their importance in determining which alternative to select. The recommended approach is to sum all the weight factors to a unity sum (1.0)[47]. In this particular trade-off study the weight factors will be assigned by the project manager.

Table 3-17: Decision matrix

Decision Criteria	Assigned weight factors
Robustness	0.2
Efficiency	0.15
Cost	0.1
Risk	0.15
Reliability	0.2
Flexibility & Expandability	0.2

3.8.7 Utility Functions

The utility function will provide a mediating capability to transform the decision criteria to a common dimensionless scale [47]. In this particular trade-off study the utility score will range between 0 and 100, 0 to 10 is poor, 11-50 is good and 51 to 100 is excellent.

3.8.8 Evaluating alternatives

In this section each of the values awarded are motivated in Table 3-18. These evaluations were the result of studying the data transmission standards and their application notes. The performances are evaluated by using the decision criteria as discussed in Section 3.8.5. The alternatives were evaluated according to their performance as shown in Table 3-19.

Table 3-18: Raw score motivation

Decision criteria	Raw scores motivation
Robustness	<p>When rating the robustness, the most important aspect to consider is the level of <i>noise immunity</i>. Thus the level of noise immunity will be rated.</p> <ol style="list-style-type: none"> 1.RS 485 and USB2 specify a physical layer specification that implements differential signalling over a twisted pair cable. This is considered extremely noise resistant for an industrial system setup. Therefore the raw score is rated excellent. 2.TIA/EIA 899 also specifies twisted pair cabling however this standard is considered more susceptible to noise, because very low voltage swings are used. Therefore the raw score rating is considerably lower. 3.IEEE 1284 also specifies twisted pair cabling, however this standard <i>is not</i> considered robust, because crosstalk and clock skew are great disadvantages of parallel communication over long distances. 4.Fibre optic is a physical medium that is considered to be noise immune. Therefore the raw score rating is very high for this alternative.
Efficiency	<p>When rating efficiency the level of <i>error detection</i> and correction implemented in the data transmission standard will be rated</p> <ol style="list-style-type: none"> 1.RS 485, TIA/EIA 899, Fibre optics and IEEE 1284 do not implement any level of error detection or correction. However if one of these electrical standards will be used, it will be used in conjunction with a protocol that implements error detection. Therefore the raw score awarded was good. 2.USB2 implements a 16 bit CRC. The error correction implemented is not that specialized and only incorporates ignoring and discarding faulty packets. Implementing CRCs are considered to be the best method to detect errors; therefore the raw score rating is excellent.
Cost	<p>When rating <i>cost</i> the cost of implementing the data transmission standards and the amount of components needed will be rated.</p> <ol style="list-style-type: none"> 1.Alternative 1 is considered more cost effective, because the transmission medium is cheap and less communication drivers are required. 2.Alternative 2 is a little more expensive, because more communication drivers are required, both ratings however is excellent. 3.TIA/EIA 899 is considered more expensive because the communication drivers required are more advanced; however some FPGAs have build in LVDS drivers. Thus the rating is still good. 4.Commercial of the shelf (COTS) boards that consists of fibre optic drivers were not found. Therefore the board must be developed, which would be considerably more expensive. Furthermore the cost will be higher because electronic/optical/electronic conversion incurs greater cost. 5.Implementation cost of USB will be more costly, because a central hub will be required and more advanced drivers.
Risk	<p>When rating <i>risk</i> the risk factor the, technical risk for the designers will be rated.</p> <ol style="list-style-type: none"> 1.The technical risk for implementing RS 485 and TIA/EIA 899 is very low on FPGAs. 2.The technical risk for IEEE 1284 is very high, because if the parallel communication link is not designed accurately the can result in being slower than serial communication. 3.The technical risk of implementing USB2 on FPGAs will be very high keeping in mind that it is very complex protocol. 4.The technical risk associated with fibre optics will also be high, keeping in mind that hardware consisting of FPGAs will need to be developed.
Reliability	<p>When rating <i>reliability</i> factors decreasing reliability will be investigated and rated, for example single</p>

	<p>points of failure, clock skew and noise susceptibility.</p> <ol style="list-style-type: none"> 1. Alternative 1,3 and 7 implement logic bus structure, therefore when the connection breaks the downstream I/O will be lost Therefore the ratings are low due to a single point of failure. 2. Alternative 2 and 6 are extremely reliable, because no single point of failure can be identified. Therefore the rating is very high. 3. USB2 also has a single point of failure, which is the hub therefore the rating is lower. 4. The immense possibility of clock skew and noise susceptibility causes the IEEE 1284 alternative's reliability to be lower.
Flexibility & Expandability	<p>When rating <i>flexibility</i> and <i>expandability</i> the alternative's ability to expand and change the system will be rated.</p> <ol style="list-style-type: none"> 1. All the alternatives are considered to be expandable and flexible except alternative 1, because the data transfer rate is restricted.

Table 3-19: Evaluation matrix

Decision Criteria	Weight	Alternative 1 (RS 485 daisy chaining)		Alternative 2 (RS 485 point-to-point)		Alternative 3 (TIA/EIA 899 daisy chaining)		Alternative 4 (USB2)		Alternative 5 (IEEE 1284)		Alternative 6 (Fibre optic point-to-point)		Alternative 7 (Fibre optics logic bus)	
		Raw ⁵ Score	Weighted ⁶ Score	Raw Score	Weighted Score	Raw Score	Weighted Score	Raw Score	Weighted Score	Raw Score	Weighted Score	Raw Score	Weighted Score	Raw Score	Weighted Score
Robustness	0.2	80	16	80	16	50	10	80	16	10	2	100	20	100	20
Efficiency	0.15	50	7.5	50	7.5	50	7.5	80	12	10	1.5	50	7.5	50	7.5
Cost	0.1	90	9	60	7	50	5	50	5	50	5	10	1	10	1
Risk	0.15	90	13.5	90	13.5	80	12	10	1.5	40	6	10	1.5	10	1.5
Reliability	0.2	50	10	90	18	50	10	50	10	20	4	90	18	50	10
Flexibility	0.2	50	10	80	16	80	16	80	16	50	10	80	16	80	16
Totals ⁷	1		0.66		0.78⁸		0.605		0.605		0.285		0.64		0.56

⁵ The raw score is awarded according the evaluation of the alternative. These scores are motivated in Table 3-19.

⁶ The weighted scores are multiplied by the weights assigned in Section 3.8.6

⁷ Totals are calculated to evaluate which alternative obtained the highest total.

⁸ Alternative 2 obtained the highest total.

3.9 Trade-off study for IF 1.0

The second trade-off study will determine the optimum data communication standard that will be implemented between the main controller (FU 1.1) and the ISensorboard (FU 1.2). This trade-off study will follow the same steps as the first. However the decision criteria, weight factors and the utility function will stay the same as in Sections 3.8.5, 3.8.6 and 3.8.7 and will not be discussed again in this section.

3.9.1 Requirements

In this section the requirements will be listed for IF1.0. These requirements will also be considered as go/no-go constraints.

3.9.1.1 Constraint 1

Requirement: Minimum data refresh rate (<i>clock frequency</i>)	20 kHz
--	--------

The term data transfer rate has already been defined explained in Section 2.7.5. This section will commence with calculating the minimum data transfer rate. As already been calculated in Section 3.8.1.2 the clocking time interval is 50 μ s. The clocking time interval will be used to calculate the data transfer rate by using (3.1). The information that must be communicated between the ISensorboard and the main controller is shown in Table 3-20. This table was obtained from the refined functional analysis.

Table 3-20: Refined functional analysis

Functional Unit	Internal communication			Functional Unit
FU 1.1 Main controller				
	F1.4 Communicate			
		F1.4.1 Transmit		
			Prompt signal	FU1.2 ISensorboard
			Error checking	FU1.2 ISensorboard
		F1.4.2 Receive		
			Rotor position values	FU1.2 ISensorboard
			Error condition	FU1.2 ISensorboard
			Error checking	FU1.2 ISensorboard

By using Table 3-20 the number of bits that must be transmitted per clock time interval between the ISensorboard and the main controller can be calculated as shown in Table 3-21.

Table 3-21: Amount of data to be communicated

Functional Unit	Internal communication			Functional Unit	Bits
FU1.1 Main controller					
	F1.4 Communicate				
		F1.4.1 Transmit	Prompt signal & Error checking	FU1.2 ISensorboard	32
		F1.4.2 Receive			
			Position value X1	FU1.2 ISensorboard	16
			Position value X2	FU1.2 ISensorboard	16
			Position value Z	FU1.2 ISensorboard	16
			Error condition	FU1.2 ISensorboard	16
			Error checking	FU1.2 ISensorboard	16
				Total number of bits to be transmitted	112

The data transfer rate⁹ can now be calculated.

The data transfer rate¹⁰ can now be calculated by using (3.3)

$$\begin{aligned} \text{Data transfer (bps)} &= 112[\text{bits}] \times 20 \times 10^3[\text{Hz}] \\ &= 2.24 \text{ Mbps} \end{aligned} \quad (3.5)$$

3.9.1.2 Constraint 2

Requirement: Communication link distance	15 m
---	------

⁹ The data transfer rate calculated exclude overhead.

¹⁰ The data transfer rate does not include overhead.

The implication of this requirement is that the selected communication method must be able to transmit the data signal 15 m without disintegration of the signal. This requirement will directly be considered as a constraint, if this constraint is not met by the listed communication methods, it will not be selected as a viable alternative.

3.9.1.3 Constraint 3

Requirement: Maximum number of slaves	1
Requirement: Maximum number of masters	1
Requirement: Communication direction	Half-duplex, bi-directional, two channels

These requirements will be directly considered as a constraint, if these constraints are not met by the listed communication methods it will not be selected as a viable alternative.

3.9.2 Identify viable data communication alternatives

Various communication methods are listed in Table 3-6, these communication methods will be narrowed down by selecting only the communication methods that adhere to the go/no go constraints. The remaining viable communication methods are listed in Table 3-24.

3.9.2.1 Screening 1

During the first screening, the following communication techniques were eliminated due to inability to reach the high data transfer required.

Table 3-22: Screening 1

1.	RS 232
2.	I2C
3.	CAN bus
4.	1-Wire
5.	SMBUS
6.	LIN Bus
7.	M Bus

3.9.2.2 Screening 2

During the second screening the following communication techniques were eliminated due to the inability to communicate over the required distance.

Table 3-23: Screening 2

1.	SPI
2.	PCI
3.	GPIB
4.	IEEE 1284
5.	Microwire
6.	Gigabit Ethernet

3.9.2.3 Screening 3

During the screening 3 RS 422 was eliminated, because of the inability to transfer data bi-directional.

3.9.2.4 Viable alternatives

The remaining alternatives are viable, but only RS 485, USB2 and Fibre optic communication will be evaluated.

Table 3-24: Viable alternatives that satisfy the go/no go constraints

1.	RS 485
2.	USB1 & USB2
3.	TIA/EIA 899
4.	TIA/EIA 644
5.	Fibre optic communication
6.	M Bus

3.9.3 Proposed communication systems

3.9.3.1 System 1

Communication system 1 proposes to use the data transmission standard RS 485 (half-duplex) which is only a physical layer specification. The specifications of RS 485 are summarized in Table 3-11. The proposed architecture is illustrated in Figure 3-19. The proposed architecture satisfies all the constraints.

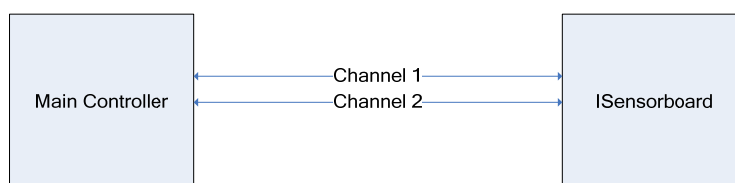


Figure 3-19: Proposed communication system 1

3.9.3.2 System 2

Communication system 2 proposes to use the communication standard USB2 which is a full interface standard. The specifications of USB2 are summarized in Table 3-13. The proposed architecture is illustrated in Figure 3-20. This specific architecture is realized by implementing a USB2 link with two repeaters to amplify the signal every five meters. The proposed architecture satisfies all the constraints.

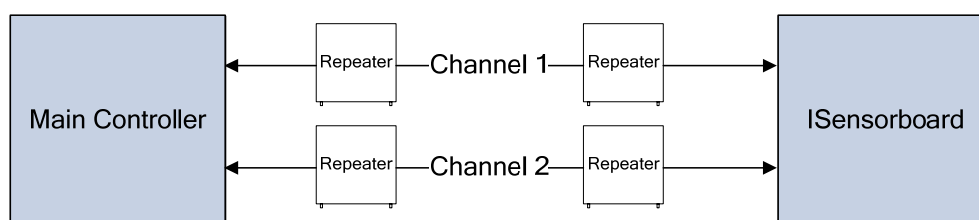


Figure 3-20: Proposed communication system 2

3.9.3.3 System 3

Communication system 3 proposes to use fibre optics to communicate between the main controller and the ISensorboard. The specifications of fibre optic communication are summarized in Table 3-15. The proposed architecture is illustrated in Figure 3-21. A point-to-point topology will be implemented with one transmit and one receive fibre for each of the channels. The proposed communication system satisfies all the constraints.

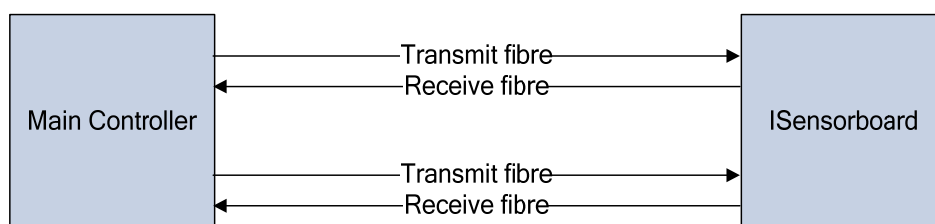


Figure 3-21: Proposed communication system 3

3.9.4 Define objectives and values

- To ensure effective communication between the ISensorboard and the main controller over a maximum distance of 15 m.
- To transmit position values from ISensorboard to the main controller.
- To refresh these values every 50 μ s.
- To receive the error condition of the ISensorboard continuously.
- To prompt the ISensorboard in the event that the sync signal is lost.
- To establish 2 communication channels.

3.9.5 Evaluate alternatives

Evaluating the alternatives work the same as discussed in Section 3.8.8. In Table 3-25 the alternatives are evaluated. The raw score given is motivated in Table 3-26.

Table 3-25: Evaluation matrix

Decision Criteria	Weight ¹¹	Alternative 1		Alternative 2		Alternative 3	
		Raw ¹² Score	Weighted Score	Raw Score	Weighted Score	Raw Score	Weighted Score
Robustness	0.2	80	16	80	16	100	20
Efficiency	0.15	50	7.5	80	12	50	7.5
Cost	0.1	60	6	10	1	40	4
Risk	0.15	90	13.5	10	1.5	10	1.5
Reliability	0.2	90	18	50	10	90	18
Flexibility	0.2	80	16	50	10	80	16
Totals	1		0.77 ¹³		0.505		0.67

¹¹ The raw score are adjusted according to these weights.

¹² The raw scores are multiplied by the weights assigned in Section 3.8.6.

Table 3-26: Raw score motivation

Decision criteria	Raw scores motivation
Robustness	<p>When rating the robustness, the most important aspect to consider is the level of <i>noise immunity</i>. Thus the level of noise immunity will be rated.</p> <ol style="list-style-type: none"> 1. RS 485 and USB2 specify a physical layer that implements differential signalling over a twisted pair cable. This is considered extremely noise resistant for an industrial system setup. Therefore the raw score is rated as excellent. 2. Fibre optic is considered to be noise immune. Therefore the raw score rating is very high.
Efficiency	<p>When rating efficiency the level of <i>error detection</i> and correction implemented in the data transmission standard will be rated.</p> <ol style="list-style-type: none"> 1. RS 485 and fibre optics do not implement any level of error detection or correction. However if one of these electrical standards will be used, it will be used in conjunction with a protocol that implements error detection. Therefore the raw score awarded was good. 2. USB2 implements a 16 bit CRC. The error correction implemented is not that specialized and only incorporates ignoring and discarding faulty packets; however the raw score awarded is still very high.
Cost	<p>When rating <i>cost</i> the cost of implementing the data transmission standards and the amount of components needed will be rated.</p> <ol style="list-style-type: none"> 1. Alternative 1 is very cost effective; therefore the rating is very high. 2. Alternative 2 is more expensive keeping in mind that repeaters were necessary for the specified distance. 3. Commercial of the shelf (COTS) boards that consisted of fibre optic drivers and an FPGA with embedded PowerPC were not found. Therefore the board must be developed, which would be considerably more expensive. Furthermore for fibre optics the cost will be higher because electronic/optical/electronic conversion is generally more expensive.
Risk	<p>When rating the <i>risk</i> factor the technical risk for the designers will be rated.</p> <ol style="list-style-type: none"> 1. The technical risk for implementing RS 485 is low. 2. The technical risk of implementing USB2 on and FPGA is higher, because it is a very complex protocol. 3. Technical risk associated with fibre optics was also higher, keeping in mind that a board consisting of very complex components would need to be developed from scratch
Reliability	<p>When rating <i>reliability</i> the amount of components necessary to implement an alternative will be investigated, because more components increase the risk of failure.</p> <ol style="list-style-type: none"> 1. Alternative 1 and 3 consists of less components resulting in the risk of failure to decrease 2. Quite a few components are used in alternative 2, increasing the risk of failure; therefore the score was rated lower.
Flexibility & Expandability	<p>When rating <i>flexibility</i> and <i>expandability</i> the alternative's ability to expand and change the system will be rated.</p> <ol style="list-style-type: none"> 1. Alternative 1 and 3 were considered to be expandable and flexible, because in both alternatives the data transfer rate and the distances can be increased. 2. Alternative 2 however requires additional hardware to increase the distance; therefore the score was rated lower.

¹³ Alternative 1 obtained the highest total.

3.10 Trade-off study for IF 1.2

Deciding which data transmission standard to implement between the main controller (FU1.1) and the motor drive unit (FU1.4) will only entail listing the requirements of the interface. The reason for this difference is, because during the first stage of the ADES, the motor drive will be a commercial of the shelf model. Thus the model that will be selected must adhere to the requirements as given in Section 3.10.1.

3.10.1 Requirements

In this section the requirements will be listed for IF1.2. These requirements will be considered as go/no go constraints, if a communication method does not meet these requirements, it cannot be listed as a viable alternative.

3.10.1.1 Constraint 1

Requirement: Minimum data refresh rate (<i>clock frequency</i>)	1 kHz
--	-------

The minimum data transfer rate calculated for a clocking frequency of 1 kHz will be considered as a go/no go constraint. If this constraint is not met by the listed communication methods, it will not be selected as a viable alternative.

Minimum data transfer rate:

The clocking time interval can be calculated by using (3.1):

$$\begin{aligned} \text{Clock interval} &= \frac{1}{1 \times 10^3} \\ &= 1 \text{ ms} \end{aligned} \quad (3.6)$$

The data transfer rate can be calculated by using (3.3). The information that must be communicated between the motor drive unit and the main controller is shown in Table 3-27. This table was obtained from the refined functional analysis.

Table 3-27: Refined functional analysis

Functional Unit	Internal communication			Functional Unit
FU 1.1 Main controller				
	F1.4			

	Communicate			
		F1.4.1 Transmit		
			Tx: PMSM speed reference	FU1.4 Motor drive unit
		F1.4.2 Receive		
			Rx: PMSM speed value	FU1.4 Motor drive unit

By using Table 3-27 the number of bits that must be transmitted per clock time interval between the ISensor board and the main controller can be calculated as shown in Table 3-28.

Table 3-28: Amount of data to be communicated

Functional Unit	Internal communication			Functional Unit	Bits
FU1.1 Main controller					
	F1.4 Communicate				
		F1.4.1 Transmit			
			Motor drive reference speed	FU1.4 Motor drive unit	16
		F1.4.2 Receive			
			Motor drive true speed value	FU1.4 Motor drive unit	16
			Error checking	FU1.4 Motor drive unit	16
				Total number of bits to be transmitted (without overhead)	48

The data transfer rate can now be calculated by using (3.3):

$$\begin{aligned}
 \text{Data transfer (bps)} &= 48[\text{bits}] \times 1 \times 10^3[\text{Hz}] \\
 &= 48 \text{ kbps}
 \end{aligned}
 \tag{3.7}$$

3.10.1.2 Constraint 2

Requirement: Communication link distance	10 m
---	------

The implication of this requirement is that the selected communication method must be able to transmit the data signal over 10 m without disintegration of the signal. This requirement will directly be considered as a constraint, if this constraint is not met by the listed communication methods, it will not be selected as a viable alternative.

3.10.1.3 Constraint 3

Requirement: Maximum number of slaves	1
Requirement: Maximum number of masters	1
Requirement: Communication direction	Bi-directional, half duplex

These requirements will be directly considered as a constraint, these constraints have to be met by the commercial of the shelf motor drive.

3.11 Trade-off study for IF 1.4

A trade-off study will not be conducted for the IF 1.4, because a data transmission standard is not going to be implemented. A CMOS digital line will be used to monitor whether the power conditioning unit is functioning correctly.

3.12 Trade-off study for IF 1.5

The fifth trade-off study will determine the optimum data transmission standard that will be implemented between the main controller (FU 1.1) and the SBC (FU 1.8).

3.12.1 Requirement

Considering that the selected SBC is a card that consists of two PMC sites, it will be necessary to identify a PMC module for the communication card. Thus it is a given that a PCI high-performance industrial bus will be implemented between the main controller and the SBC.

3.13 Trade-off study for IF 1.5

A trade-off study will not be conducted for the IF 1.5, because a data transmission standard is not going to be implemented. A CMOS digital line will be used to route the synchronization signal to each of the functional units present in the control cycle.

3.14 Trade-off study for external interfaces

This trade-off study will determine the optimum data transmission standard that will be implemented between the SBC and the external interfaces (FU 6.0, FU 8.0). The same design process as specified in Section 3.5 will be followed.

3.14.1 Interface identification

Figure 3-22 displays the external ADES interfacing entities.

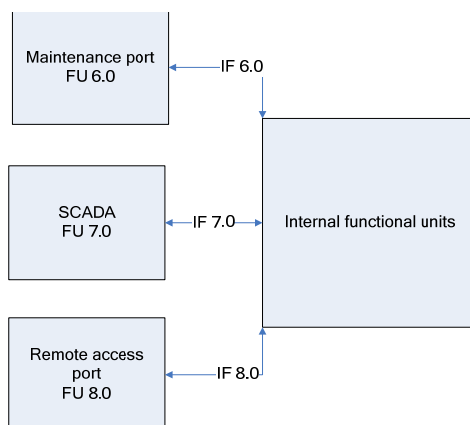


Figure 3-22: External interface diagram

3.14.2 Requirements for IF6.0 (Maintenance port)

In this section the requirements will be listed for IF6.0. These requirements will be considered to be go/no go constraints, if a communication method does not meet these requirements, it cannot be listed as a viable alternative. The constraints are listed in Table 3-29.

Table 3-29: Constraints

F 1.4.4 - Communicate via maintenance port	
Description	Specification
Bit rate	>30 Mbps
Maximum Information Refresh rate	20 kHz
Connection type	Point-Point
Maximum distance between ADES and connecting device	2 m
Specified Protocol	Standardized protocol ¹⁴

The data transfer rate was obtained by using (3.1) and (3.3). The maximum data that must be communicated between the ADES and the maintenance port per time interval is listed in Table 3-30.

Table 3-30: Data to be communicated

ADES	External Communication			Functional Unit
	Transmit			
		Communicate		
			Rotor speed	Maintenance port
			Status signals	Maintenance port
			System mode and state	Maintenance port
			Temperatures	Maintenance port
			Monitor 10 EM currents	Maintenance port
			Monitor 5 rotor positions	Maintenance port
			Pressures and flow rates	Maintenance port

¹⁴ It was decided to implement only standardized, full interface data transmission standards for the external interfaces, the reason being that these standards have been tried and tested and is compatible with other systems for example PLCs and SCADAs that is commonly used in the industrial setup.

By using Table 3-30 the maximum number of bits that must be transmitted per clock time interval between the ADES and the maintenance port can be calculated as shown in Table 3-31.

Table 3-31: Amount of data to be communicated

ADES	External Communication			Bits
	Transmit			
		Communicate		
			Rotor speed	16
			Status signals (13)	208
			System mode	16
			System state	16
			Pressures and flow rates (10)	160
			Monitor 10 EM coil currents	160
			Monitor 5 rotor positions	80
			Total bits (without overhead)	656

The data transfer rate can now be calculated.

$$\begin{aligned} \text{Data transfer (bps)} &= 656[\text{bits}] \times 20 \times 10^3[\text{Hz}] \\ &= 13.12 \text{ Mbps} \end{aligned} \quad (3.8)$$

3.14.3 Requirements for IF 7.0 (ADES and SCADA)

A trade-off study will not be conducted to determine the optimum data communication standard that will be implemented between the ADES (FU 1.0) and the SCADA (FU 7.0). The Profibus DP protocol will be implemented to establish bi-directional communication in order to guarantee compatibility with the PLC installed on site. All the SCADA specifications are listed in Table 3-32. The main goal of the SCADA will be to issue commands to the ADES, examples of these commands are, power up, power down and download the operation history. For more information about the SCADA commands refer to the "Systems requirement specification for the ADES" document.

Table 3-32: SCADA specifications

Communicate via SCADA interface	
Description	Specification
Specified protocol	Profibus DP
Bit rate	12 Mbps
Maximum information refresh rate	1 Hz
connection type	Multidrop down configuration
Maximum distance	100 m

3.14.4 Requirements for IF8.0 (Remote access)

In this section the requirements will be listed for IF8.0. These requirements will be considered to be go/no go constraints, if the proposed communication method does not meet these requirements, it cannot be listed as a viable alternative. The constraints are listed in Table 3-33. The data that must be communicated between the remote access port and the main controller is the same as the data that must be communicated between the main controller and the maintenance port.

Table 3-33: Remote access constraints

Remote access constraints	
Description	Constraint
Bit rate	No specific requirement
Maximum information refresh rate	No specific requirement
Connection type	No specific requirement
Specified protocol between ADES and server	Standardized protocol
Distance between ADES units and server	100 m
Maximum nodes	1

3.14.5 Identifying viable data communication systems & screening alternatives

There exist countless viable alternatives for the external interfaces. However these alternatives can be narrowed down to the interfaces available on standard laptops and servers. These interfaces are;

1. Ethernet port
2. USB1 or USB2 ports
3. Serial ports (RS 232)
4. Parallel ports

Out of these viable alternatives, Ethernet and USB will be investigated.

3.14.6 Proposing different communication systems

3.14.6.1 System 1

System 1 proposes to use the USB2 protocol for both the remote access port (IF 8.0) and the maintenance port (IF 6.0). The specifications for the USB2 standard are listed in Table 3-13. The required data transfer rate will certainly not exceed the maximum data transfer rate specified for USB2 when the overhead is added. The proposed architecture for communication system 1 is illustrated in Figure 3-23 .

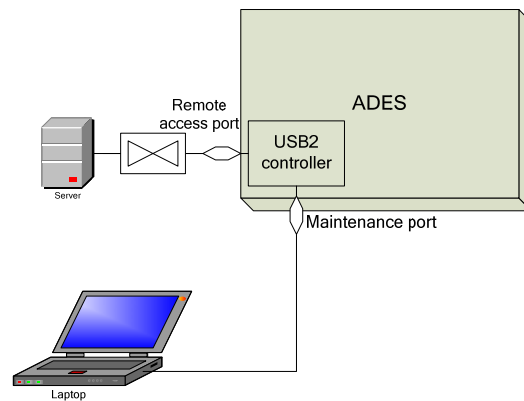


Figure 3-23: Proposed communication system 1

Figure 3-23 illustrates how the ADES will communicate with the maintenance port and the remote access port. The data that must be communicated over the remote access port and the maintenance port will be situated in registers on a common high-speed USB2 controller. The USB2 controller will not only have access to the necessary data, but will also construct the correct USB2 frames. The remote access port will communicate the correct data to a remote access server. Repeaters will be necessary due to the distance between the ADES and the server.

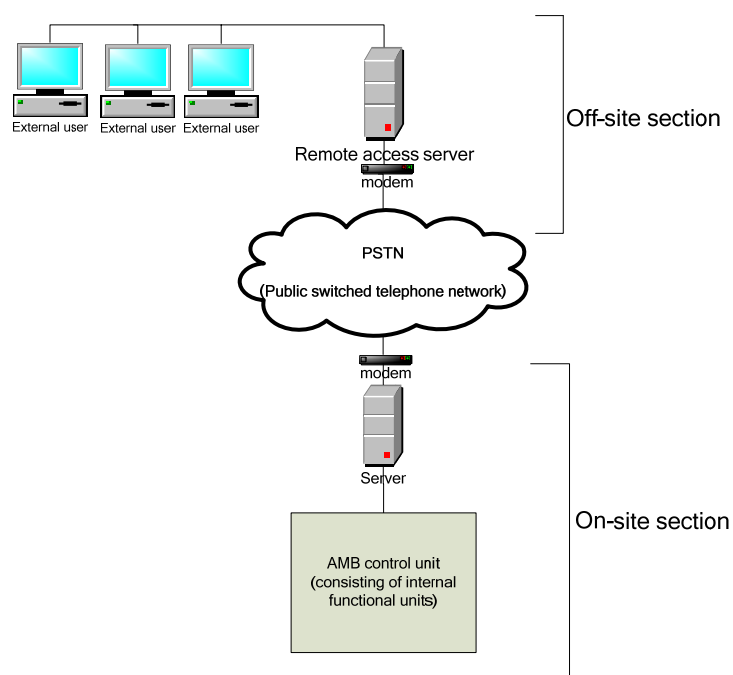


Figure 3-24: Proposed interface with the remote access server

The remote access port will connect to a server by using a point-to-point connection. At the other side the server will connect through a network interface card to modems which dial-in/out of the wide area network. The remote access server will allow external users, not situated on-site to connect into the AMB control box via an ISDN or ADSL connection as shown in Figure 3-24. The remote access servers will support more than one user. User authentication will also be implemented.

3.14.6.2 System 2

System 2 proposes to use the Fast Ethernet protocol for both the remote access port (IF 8.0) and the maintenance port (IF 6.0). The specifications of Fast Ethernet are listed in Table 3-34. Original Ethernet was ruled out due to data transfer rate limitations.

Table 3-34: Fast Ethernet specifications [48]

Topologies	Maximum cable length	Maximum data transfer rate
Logic bus Star Point-to-point	Differs according to the selected cable ¹⁵ .	100 Mbps

The proposed architecture for communication system 2 is illustrated in Figure 3-25.

¹⁵ 100Base-TX standard (category 5 UTP cable) is predominant and is limited to 100 m.

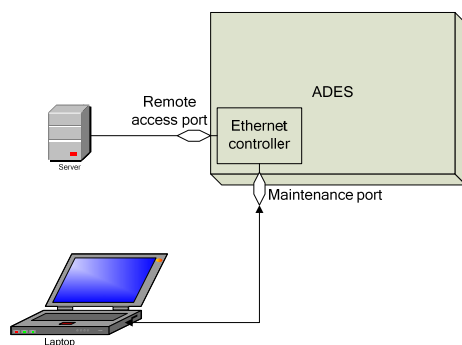


Figure 3-25: Proposed communication system 2

Figure 3-25 illustrates how the ADES will communicate with a laptop via the maintenance port and a server via a remote access port. The data that must be communicate over the remote access port and the maintenance port will be situated in registers on a common Ethernet controller. The Ethernet controller will not only have access to the necessary data, but will also construct the correct Ethernet frames. The method that will be used to interface the ADES with the remote access server will be exactly the same as in Figure 3-24.

3.14.6.3 System 3

System 3 proposes to use the Fast Ethernet protocol for the remote access port (IF 8.0) and USB2 protocol for the maintenance port (IF 6.0).The specifications for the USB2 protocol and the Fast Ethernet protocol are listed in Table 3-13 and Table 3-34. The proposed communication structure is shown in Figure 3-26.

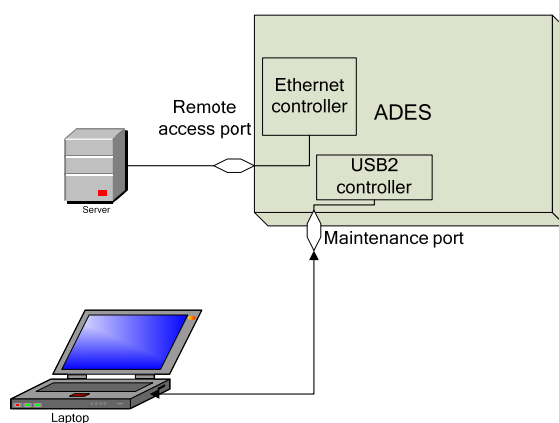


Figure 3-26: Proposed communication system 3

Figure 3-26 illustrates how the ADES will communicate with the maintenance port and the remote access port. The data that must be communicated over the remote access port will be situated in registers on the Ethernet controller. This controller will not only have access to the necessary data, but will also construct the correct Ethernet frames. The data that must be communicated over the maintenance port will be situated in registers on the USB2 controller; this controller will also construct the correct USB2 frames. The method that will be used to interface the ADES unit with the remote access server will be similar as shown in Figure 3-24.

3.14.7 Define objectives and values

- To ensure effective bi-directional communication between the ADES and a laptop
- To ensure effective bi-directional communication between the ADES and the remote access server.
- To implement communication protocols that is compatible with the industrial system setup.

3.14.8 Decision criteria

Table 3-35: Decision criteria

Decision Criteria	Criteria description
Robustness	Noise immunity of the data transmission standard.
Efficiency	Level of error detection and correction implemented in the data transmission standard.
Cost	Cost of implementing the selected data transmission standard.
Risk	Technical implementation risk.
Reliability	The reliability of various components used to implement the protocol.
Flexibility & Expandability	The ability to add new functions without changing hardware.
Compatibility	Compatibility with the industrial system setup.

3.14.9 Assign Weight Factors

Table 3-36: Decision matrix

Decision Criteria	Assigned Weight Factors
Robustness	0.05
Efficiency	0.05
Cost	0.15

Risk	0.15
Reliability	0.15
Flexibility & Expandability	0.20
Compatibility	0.25

3.14.10 Utility Functions

The same utility function will be used as documented in Section 3.8.7.

3.14.11 Evaluate Alternatives

In this section each of the alternatives were evaluate according to their performance. These evaluations were the result of studying application notes for theoretical estimations. Each of the raw scores awarded is motivated in Table 3-38.

Table 3-37: Evaluation matrix

Decision criteria	Weight	Alternative 1 (USB2)		Alternative 2 (Fast Ethernet)		Alternative 4 (USB2 and Fast Ethernet)	
		Raw Score	Weighted Score	Raw Score	Weighted Score	Raw Score	Weighted Score
Robustness	0.05	80	4	80	4	80	4
Efficiency	0.05	80	4	80	4	80	4
Cost	0.15	20	3	60	9	10	1.5
Risk	0.15	50	7.5	50	7.5	0	0
Reliability	0.15	10	1.5	80	12	50	7.5
Flexibility & Expandability	0.2	80	16	80	16	80	16
Compatibility	0.25	90	22.5	90	22.5	90	22.5
Total			0.56		0.75 ¹⁶		0.59

¹⁶ Alternative 2 obtained the highest total.

Table 3-38: Raw score motivation

Decision criteria	Raw scores motivation
Robustness	<p>When rating the robustness, the most important aspect to consider is the level of <i>noise immunity</i>. Thus the level of <i>noise immunity</i> will be rated.</p> <ol style="list-style-type: none"> 1. All the systems were rated the same, because each of the communication systems implements protocols that are considered to be exceedingly noise immune.
Efficiency	<p>When rating efficiency the level of <i>error detection</i> and correction implemented in the data transmission standard will be rated.</p> <ol style="list-style-type: none"> 1. Each of the communication systems implements advanced error detection. A level of error correction is also implemented, although it is not that advanced. Therefore all the systems were awarded an excellent rating.
Cost	<p>When rating <i>cost</i> the cost of implementing the data transmission standards and the amount of components needed will be investigated.</p> <ol style="list-style-type: none"> 1. Implementing USB2 will be costly considering that repeaters will be essential in order to realize the required distance; therefore the raw score given was very low. 2. Alternative 3 will be extremely costly, considering that individual hardware will be required for the maintenance port and the remote access port.
Risk	<p>When rating the <i>risk</i> factor the technical risk for the designers will be rated.</p> <ol style="list-style-type: none"> 1. Technical risk associated with implementing each of the alternatives are high, however alternative 4 is much higher considering that two different protocols must be mastered.
Reliability	<p>When rating <i>reliability</i> the amount of components necessary to implement an alternative will be investigated, because more components increase the risk of failure.</p> <ol style="list-style-type: none"> 1. Alternative 1 requires more components (hubs) reducing reliability significantly. 2. Alternative 2 will not require the same amount of components, increasing reliability. 3. Alternative 3 will require more component, once again reducing reliability.
Flexibility & Expandability	<p>When rating <i>flexibility</i> and <i>expandability</i> the alternative's ability to expand and change the system will be rated. The ability to add new functions without changing hardware.</p> <ol style="list-style-type: none"> 1. All the alternatives are considered to be extremely expandable and flexible.
Compatibility	<p>Compatibility with the industrial system setup.</p> <ol style="list-style-type: none"> 1. All the alternatives implement standardized protocol which is compatible with industrial system setups, therefore the ratings are high.

3.15 Final communication system

After discussing the best system architecture for the ADES and conducting a detailed trade-off study for each of the interfaces, the top-level functional architecture for the communication system was obtained as illustrated Figure 3-27.

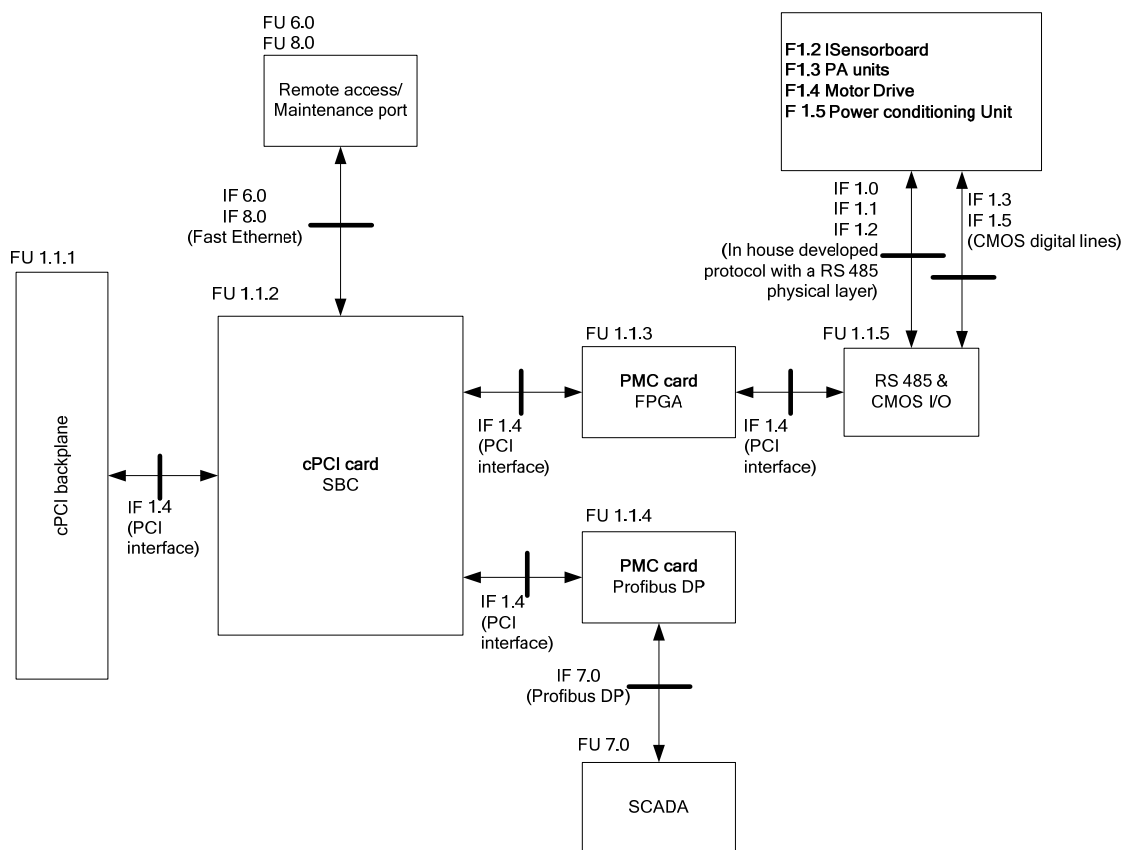


Figure 3-27: Top-level functional architecture of the communication sub-system

3.15.1 Internal interfaces

It was decided to develop an in-house protocol for the internal interfaces of the ADES. Industrial systems often make use of in-house developed protocols for internal system communication. This is done where no human interfaces are present and system to system compatibility is not necessary. Implying that no commercial of the shelf systems will need to interface with the in-house developed protocol. Furthermore this protocol will only be used for the *direct control cycle* of the ADES between the functional units developed by McTronX research group.

Two of the advantages of developing an in house protocol are; no unnecessary futures are added and the protocol can be developed for the *specific* needs of an AMB application.

The physical layer of the protocol will use the RS 485 data transmission standard as indicated by the trade-off studies and the remainder of the protocol – from here on referred to as the ADES digiComm protocol - will be designed in Chapter 4.

3.15.2 External interfaces

For the external interfaces only standardized protocols will be used, keeping in mind that the external interfaces must be *compatible* with commercial off the shelf products that make use of *only* standardized protocols.

It was decided to use *Fast Ethernet* for both the remote access port and the maintenance port. Fast Ethernet is a standardized protocol and every laptop or PC consists of an Ethernet port. Profibus DP was selected for the SCADA interface, because commercial off the shelf SCADA systems make use of the Profibus DP fieldbus for communication.

3.16 Conclusion

The aim of this chapter was to determine the requirements of the ADES that were applicable to the development of the communication sub-system of the ADES. After the necessary requirements were obtained the system design commenced. This lead to the selection of the correct data transmission standard for each communication interfaces as well as development of the top-level functional architecture of the communication sub-system. Now it is possible to proceed to transmission line development, protocol development and hardware selection.

