



# A communication sub-system for the ADES

REPORT NO.: No.1

AUTHOR(S): Elsebi van Sittert

DATE: 21 October 2009

ACCESSIBILITY: Internal

DISTRIBUTION: Enter distribution list.



# DECLARATION

I hereby declare that all the material incorporated in this thesis is my own original unaided work except where specific reference is made by name or in the form of a numbered reference. The work herein has not been submitted for a degree at another university.

Signed:

---

Elsebi van Sittert



# SUMMARY

The McTronX research group has conducted extensive research concerning Active Magnetic Bearings (AMBs). This research involved the establishment of an advanced AMB laboratory to aid in assisting industries that implement AMBs in their applications. This year the McTronX group's focus shifted toward the development of an AMB system to be implemented in the Pebble Bed Modular Reactor (PBMR). The AMB system was designed to be used in a helium blower application. This involved the development of both the mechanical and the electronic components.

The main goal of this AMB system was to develop a completely digital integrated controller which is responsible for the control of the AMB system, from here on referred to as the AMB drive and electronic system (ADES). The need arose for a totally digital system to increase the reliability and robustness of the ADES. These requirements are crucial in a nuclear environment. In order to develop a totally digital system a new issue had to be addressed. This involved the implementation of digital communication.

This project involved the development of a communication sub-system for the ADES. The communication system was divided into two sections, the internal and external communication system. The various interfaces were identified as well as their specifications formulated. The optimum solution was then selected for each of the interfaces by using a design process that involved comprehensive trade-off studies.

The external communication system and the internal communication system were specified and the necessary hardware was procured. An in-house developed protocol was developed and implemented between the internal functional units of the ADES. The designed protocol adhered to the specific needs of an AMB application.

The protocol was extensively tested by carrying out verification and validation tests and evaluation plans. The test and evaluation plans for verification were carried out by making use of simulations and laboratory experiments. Validation of the in-house developed protocol was carried out by analyzing the internal communication system whilst the ADES was controlling the bearing module. During this phase the communication system was also subjected to error conditions.

The protocol proved to be completely functional, robust and reliable, meeting the performance specifications and the requirements. During this project a foundation was laid for digital communication in AMB systems in the McTronX research group.



# ACKNOWLEDGEMENTS

*I would like to acknowledge the following people:*

- *My loving husband (and colleague), Gordon Gadney, for all his support, encouragement and advice during the good times and the tough times. He is my **inspiration** and without him this would certainly not have been possible.*
- *My two supervisors, Prof. G. van Schoor and Prof S.R. Holm for their guidance.*
- *Jacques Jansen van Rensburg my assistant supervisor.*
- *Rikus le Roux my dedicated colleague who fought this battle with me every step of the way!*
- *Andre Niemann and Dewald Herbst my colleagues and co-workers on the ADES project.*
- *Eugen Ranft my project manager.*
- *Jannik Bessinger and Kristoff Vosloo for their work on the RDS.*
- *My family for their ongoing support through my studies.*





***Soli Deo Gloria***

*“but those who hope in the Lord will renew their strength. They will soar on wings like eagles; they will run and not grow weary, they will walk and not be faint. Isaiah 41:31”*



# Contents

<b>A communication sub-system for the ADES.....</b>	<b>1</b>
<b>DECLARATION .....</b>	<b>iii</b>
<b>SUMMARY .....</b>	<b>v</b>
<b>ACKNOWLEDGEMENTS.....</b>	<b>vii</b>
<b>List of figures .....</b>	<b>xx</b>
<b>List of tables .....</b>	<b>xxvii</b>
<b>List of abbreviations.....</b>	<b>xxxi</b>
<b>List of symbols.....</b>	<b>xxxiii</b>
<b>Chapter 1 .....</b>	<b>1</b>
<b>1 Introduction .....</b>	<b>1</b>
<b>1.1 The digital phenomenon.....</b>	<b>1</b>
<b>1.2 Background.....</b>	<b>2</b>
1.2.1 AMBs .....	3
1.2.2 ADES .....	4
1.2.3 Proposed system structure .....	4
<b>1.3 Problem statement.....</b>	<b>5</b>
<b>1.4 Issues to be addressed and methodology .....</b>	<b>6</b>
1.4.1 Literature study .....	6
1.4.2 Conceptual design.....	7
1.4.3 Detailed design .....	7
1.4.4 Verification and validation.....	8
<b>1.5 Dissertation layout .....</b>	<b>8</b>
<b>1.6 Conclusion .....</b>	<b>9</b>
<b>Chapter 2 .....</b>	<b>11</b>

<b>2</b>	<b>Literature Study .....</b>	<b>11</b>
2.1	Introduction .....	11
2.2	Electronic communication systems .....	12
2.3	Analogue transmission .....	13
2.4	Digital communication .....	14
2.5	Analogue versus digital communication .....	14
2.6	Analysing and designing a communication system .....	14
2.7	Digital communication system .....	15
2.7.1	Digital transmission .....	15
2.7.2	Data transmission .....	17
2.7.3	Data transmission topologies .....	19
2.7.4	Electrical interface circuitry .....	20
2.7.5	Data signalling rate, data signalling frequency and data transfer rate .....	22
2.7.6	Data transmission standard .....	23
2.8	Open Systems Interconnection (OSI) reference model .....	24
2.9	Data transmission standards .....	25
2.9.1	RS 232 .....	26
2.9.2	RS 422 .....	26
2.9.3	RS 485 .....	28
2.9.4	Serial peripheral interface (SPI) .....	29
2.9.5	Universal serial bus (USB) .....	30
2.9.6	Low voltage differential signalling (LVDS), LVDS – multi point (LVDM) and .....	31
	Multi-point LVDS (M-LVDS) .....	31
2.9.7	PCI and CompactPCI (Peripheral Component Interconnection) .....	33
2.9.8	Comparing local bus solutions .....	33
2.9.9	Profibus .....	37
2.10	Limitations of busses .....	38

2.10.1	Attenuation.....	39
2.10.2	Jitter .....	39
2.10.3	Drift.....	40
<b>2.11</b>	<b>Transmission lines .....</b>	<b>40</b>
2.11.1	Types of transmission lines .....	40
2.11.2	Transmission line modelling.....	43
<b>2.12</b>	<b>Communication systems evaluation .....</b>	<b>46</b>
2.12.1	Physical layer .....	46
2.12.2	Protocol analysis (data link layer) .....	49
2.12.3	Transmission line analysis.....	50
<b>2.13</b>	<b>Critical literature review .....</b>	<b>50</b>
<b>2.14</b>	<b>Conclusion .....</b>	<b>52</b>
	<b>Chapter 3 .....</b>	<b>53</b>
<b>3</b>	<b>Conceptual design of the total communication system .....</b>	<b>53</b>
<b>3.1</b>	<b>Introduction .....</b>	<b>53</b>
<b>3.2</b>	<b>ADES requirements overview.....</b>	<b>53</b>
<b>3.3</b>	<b>ADES architecture options.....</b>	<b>54</b>
3.3.1	Pros vs. Cons .....	58
3.3.2	Final architecture selection.....	58
<b>3.4</b>	<b>Communication system requirements.....</b>	<b>60</b>
<b>3.5</b>	<b>Design process .....</b>	<b>60</b>
<b>3.6</b>	<b>Internal interface identification.....</b>	<b>61</b>
<b>3.7</b>	<b>Engineering trade-off study.....</b>	<b>61</b>
<b>3.8</b>	<b>Trade-off study for IF1.1.....</b>	<b>62</b>
3.8.1	Requirements .....	62
3.8.2	Identify viable data communication alternatives.....	65
3.8.3	Proposed communication systems.....	67

3.8.4	Define objectives and values .....	71
3.8.5	Decision criteria .....	71
3.8.6	Assign weight factors.....	72
3.8.7	Utility Functions .....	72
3.8.8	Evaluating alternatives .....	72
<b>3.9</b>	<b>Trade-off study for IF 1.0.....</b>	<b>76</b>
3.9.1	Requirements .....	76
3.9.2	Identify viable data communication alternatives.....	78
3.9.3	Proposed communication systems.....	80
3.9.4	Define objectives and values .....	81
3.9.5	Evaluate alternatives .....	81
<b>3.10</b>	<b>Trade-off study for IF 1.2.....</b>	<b>83</b>
3.10.1	Requirements .....	83
<b>3.11</b>	<b>Trade-off study for IF 1.4.....</b>	<b>85</b>
<b>3.12</b>	<b>Trade-off study for IF 1.5.....</b>	<b>85</b>
3.12.1	Requirement .....	85
<b>3.13</b>	<b>Trade-off study for IF 1.5.....</b>	<b>86</b>
<b>3.14</b>	<b>Trade-off study for external interfaces .....</b>	<b>86</b>
3.14.1	Interface identification .....	86
3.14.2	Requirements for IF6.0 (Maintenance port) .....	86
3.14.3	Requirements for IF 7.0 (ADES and SCADA).....	88
3.14.4	Requirements for IF8.0 (Remote access).....	89
3.14.5	Identifying viable data communication systems & screening alternatives.....	89
3.14.6	Proposing different communication systems .....	90
3.14.7	Define objectives and values .....	93
3.14.8	Decision criteria .....	93
3.14.9	Assign Weight Factors .....	93

3.14.10	Utility Functions .....	94
3.14.11	Evaluate Alternatives .....	94
<b>3.15</b>	<b>Final communication system.....</b>	<b>95</b>
3.15.1	Internal interfaces .....	96
3.15.2	External interfaces .....	97
<b>3.16</b>	<b>Conclusion .....</b>	<b>97</b>
<b>Chapter 4</b>	<b>.....</b>	<b>99</b>
<b>4</b>	<b>ADES internal digital communication system design .....</b>	<b>99</b>
<b>4.1</b>	<b>Introduction .....</b>	<b>99</b>
<b>4.2</b>	<b>Hardware.....</b>	<b>100</b>
4.2.1	Master node (PMC module).....	100
4.2.2	AXM-D03 digital mezzanine module .....	101
4.2.3	SCSI cable.....	101
4.2.4	Termination panel .....	102
4.2.5	SBC (cPCI module) .....	102
4.2.6	Profibus option.....	103
<b>4.3</b>	<b>Protocol functioning.....</b>	<b>104</b>
<b>4.4</b>	<b>Internal communication data flow path.....</b>	<b>105</b>
<b>4.5</b>	<b>Communication timing .....</b>	<b>105</b>
<b>4.6</b>	<b>Protocol layers .....</b>	<b>106</b>
4.6.1	Physical layer .....	107
4.6.2	Electrical specifications .....	107
4.6.3	Mode.....	107
4.6.4	Cable selection.....	107
4.6.5	Grounding .....	108
4.6.6	Drivers.....	109
4.6.7	Termination options .....	110

4.6.8	Biasing .....	110
4.6.9	Isolation options.....	112
4.6.10	Connector types and pin connections.....	112
4.6.11	Encoding .....	112
<b>4.7</b>	<b>Data link layer.....</b>	<b>113</b>
4.7.1	Framing .....	113
4.7.2	Medium access control.....	115
4.7.3	Error detection .....	115
4.7.4	Error correction.....	116
<b>4.8</b>	<b>Protocol Implementation.....</b>	<b>116</b>
<b>4.9</b>	<b>Basic functional blocks.....</b>	<b>118</b>
4.9.1	Design of UART receiver entity.....	118
4.9.2	Design of UART transmit entity.....	119
4.9.3	First In First Out (FIFO) .....	119
4.9.4	Dual Port Ram (DPR).....	120
4.9.5	CRC function.....	121
<b>4.10</b>	<b>Slave nodes .....</b>	<b>124</b>
<b>4.11</b>	<b>Communication control.....</b>	<b>125</b>
<b>4.12</b>	<b>ISensorboard and main controller interconnection .....</b>	<b>125</b>
4.12.1	DPR.....	126
4.12.2	UART- top level modules .....	126
4.12.3	UART controller module (ISensorboard).....	126
4.12.4	UART controller module (Main controller).....	127
4.12.5	Communication controller modules .....	127
<b>4.13</b>	<b>ISensorboard communication controller .....</b>	<b>127</b>
4.13.1	TX state machine.....	127
4.13.2	RX state machine.....	130



<b>4.14</b>	<b>Main controller communication controller.....</b>	<b>132</b>
4.14.1	Main controller state machine.....	132
<b>4.15</b>	<b>Power amplifier and Main controller interconnection.....</b>	<b>133</b>
4.15.1	DPRs .....	134
4.15.2	UART top-levels .....	134
4.15.3	UART controller (main controller).....	134
4.15.4	UART controller (power amplifiers).....	135
4.15.5	Communication controller modules .....	135
<b>4.16</b>	<b>Conclusion .....</b>	<b>135</b>
	<b>Chapter 5 .....</b>	<b>137</b>
<b>5</b>	<b>Verification and validation of the communication sub-system .....</b>	<b>137</b>
<b>5.1</b>	<b>Introduction .....</b>	<b>137</b>
<b>5.2</b>	<b>Test and evaluation plans .....</b>	<b>139</b>
<b>5.3</b>	<b>Test and evaluation plan for verification.....</b>	<b>139</b>
<b>5.4</b>	<b>Physical layer verification.....</b>	<b>139</b>
<b>5.5</b>	<b>Electrical standard - and cable selection .....</b>	<b>140</b>
5.5.1	Waveform .....	141
5.5.2	Eye diagrams .....	144
5.5.3	Characteristic impedance and termination.....	150
<b>5.6</b>	<b>Data link layer verification.....</b>	<b>152</b>
5.6.1	Transmission parameters .....	153
5.6.2	Error modules .....	159
5.6.3	ISensorboard and main controller interconnection .....	162
5.6.4	Error conditions .....	166
5.6.5	Communication timing & synchronization .....	169
<b>5.7</b>	<b>Test and evaluation plan for validation .....</b>	<b>171</b>
<b>5.8</b>	<b>Physical layer validation .....</b>	<b>171</b>

5.8.1	Eye diagram construction.....	171
5.8.2	Eye diagram construction and measurements .....	172
5.8.3	Eye measurement conclusion.....	178
5.8.4	Impedance mismatch .....	179
<b>5.9</b>	<b>Data link layer – Lower level assembly .....</b>	<b>181</b>
5.9.1	Validating framing format .....	181
5.9.2	Validating data frames.....	182
5.9.3	Validating the CRC controller .....	185
5.9.4	Validation under error conditions.....	188
5.9.5	Validating timing and synchronization.....	190
<b>5.10</b>	<b>Communication controllers and validation.....</b>	<b>193</b>
5.10.1	Data Value estimation.....	193
<b>5.11</b>	<b>Analogue vs. Digital.....</b>	<b>199</b>
<b>5.12</b>	<b>Communication system validation – highest level of assembly .....</b>	<b>201</b>
<b>5.13</b>	<b>Conclusion .....</b>	<b>204</b>
	<b>Chapter 6 .....</b>	<b>205</b>
<b>6</b>	<b>Conclusions and recommendations .....</b>	<b>205</b>
<b>6.1</b>	<b>Conclusions .....</b>	<b>205</b>
6.1.1	The communication sub-system design for the ADES.....	205
6.1.2	Analysis of the designed ADES digiComm protocol .....	206
<b>6.2</b>	<b>Recommendations for future work .....</b>	<b>207</b>
6.2.1	Motor drive.....	207
6.2.2	Implementation of external communication architecture .....	208
6.2.3	Standardizing the ADES digiComm protocol .....	208
<b>6.3</b>	<b>Possible improvements to the internal communication system.....</b>	<b>209</b>
6.3.1	BERT (Bit error rate tester) .....	209
6.3.2	Waveforms.....	209

6.3.3	Implementation of isolated drivers.....	209
6.3.4	Design of impedance matching circuit.....	209
6.3.5	Error correction.....	209
6.4	Closure.....	209
7	<b>Bibliography</b> .....	<b>211</b>
	<b>Appendix A</b> .....	<b>217</b>
1	<b>Appendix A.1: Photos of the completed system</b> .....	<b>217</b>
	<b>Appendix B: Data CD</b> .....	<b>219</b>
1	<b>Appendix B.1: System requirements specification</b> .....	<b>219</b>
2	<b>Appendix B.2: Communication drivers data sheets</b> .....	<b>219</b>
3	<b>Appendix B.3: CRC article</b> .....	<b>219</b>
4	<b>Appendix B.4: VHDL code</b> .....	<b>219</b>
5	<b>Appendix B.5: MATLAB® code</b> .....	<b>219</b>
6	<b>Appendix B.6: Example of Modelsim® test benches</b> .....	<b>219</b>
7	<b>Appendix B.7: Hardware guides</b> .....	<b>219</b>
	<b>Appendix C</b> .....	<b>221</b>
1	<b>Appendix C.1: State machine of the UART receiver</b> .....	<b>221</b>
2	<b>Appendix C.2: State machine of the UART transmitter</b> .....	<b>224</b>
3	<b>Appendix C.3: Power amplifier communication controller</b> .....	<b>226</b>
4	<b>Appendix C.4: Main controller communication controller</b> .....	<b>228</b>

## List of figures

Figure 1-1: The basic operating principle of AMBs [8].....	3
Figure 1-2: dSPACE® system configuration.....	4
Figure 1-3: Proposed system configuration and definition of the scope of this project .....	5
Figure 2-1: Model of an electronic communication system [16]. .....	12
Figure 2-2: Analogue signal and baseband transmission [15].....	13
Figure 2-3: Analogue transmission using modulation and demodulation [15].....	13
Figure 2-4: Digital signal transmitted over a digital channel [15] .....	14
Figure 2-5: Asynchronous communication.....	16
Figure 2-6: Synchronous transmission.....	16
Figure 2-7: Single-ended transmission .....	20
Figure 2-8: Differential mode signalling.....	20
Figure 2-9: Differential transmission .....	21
Figure 2-10: Balanced interface circuitry .....	27
Figure 2-11: Bus topology.....	29
Figure 2-12: Full-duplex bus structure for RS 485 [23].....	29
Figure 2-13: SPI configuration .....	30
Figure 2-14: USB system architecture .....	31
Figure 2-15: Signalling rate vs. cable length [14].....	39
Figure 2-16: Jitter.....	40
Figure 2-17: A coaxial cable.....	41
Figure 2-18: A two-wire transmission line .....	42
Figure 2-19: Unshielded twisted pair.....	42
Figure 2-20: Shielded twisted pair.....	42
Figure 2-21: A microstrip transmission line.....	43
Figure 2-22: Unit cell representation of a transmission line .....	44

Figure 2-23: Eye diagram.....	46
Figure 2-24: Data stream with jitter [45].....	47
Figure 2-25: Sampling point variation [45] .....	48
Figure 2-26: BER graph (bathtub plot) [45] .....	48
Figure 2-27: Modelsim® simulation design.....	49
Figure 2-28: Digital waveform simulation .....	50
Figure 3-1: Interfacing entities of the ADES. ....	54
Figure 3-2: Architecture 1 .....	55
Figure 3-3: Architecture 2 .....	55
Figure 3-4: Architecture 3 .....	56
Figure 3-5: Architecture 4 .....	56
Figure 3-6: Architecture 5 .....	56
Figure 3-7: Architecture 6 .....	57
Figure 3-8: Architecture 7 .....	57
Figure 3-9: Architecture 8 .....	57
Figure 3-10: Selected system architecture. ....	59
Figure 3-11: Design process [47].....	60
Figure 3-12: Internal interface identification.....	61
Figure 3-13: Proposed communication system 1.....	67
Figure 3-14: Proposed communication system 2.....	68
Figure 3-15: Proposed communication system 4.....	69
Figure 3-16: Proposed communication system 5.....	70
Figure 3-17: Proposed communication system 6.....	70
Figure 3-18: Proposed communication system 7.....	71
Figure 3-19: Proposed communication system 1.....	80
Figure 3-20: Proposed communication system 2.....	80
Figure 3-21: Proposed communication system 3.....	81

Figure 3-22: External interface diagram .....	86
Figure 3-23: Proposed communication system 1.....	90
Figure 3-24: Proposed interface with the remote access server .....	91
Figure 3-25: Proposed communication system 2.....	92
Figure 3-26: Proposed communication system 3.....	92
Figure 3-27: Top-level functional architecture of the communication sub-system .....	96
Figure 4-1: General overview of the master node.....	100
Figure 4-2: AXM-D03 mezzanine module.....	101
Figure 4-3: SCSI cable with connector .....	102
Figure 4-4: Termination panel.....	102
Figure 4-5: Single Board Computer (SBC).....	103
Figure 4-6: Profibus card .....	103
Figure 4-7: The communication structure of the system.....	104
Figure 4-8: Communication data path.....	105
Figure 4-9: System timing.....	106
Figure 4-10: Interconnection media - BLDN9841 .....	108
Figure 4-11: Grounding policy [52] .....	109
Figure 4-12: Failsafe biasing schematic [12].....	111
Figure 4-13: Fail-safe biasing circuit [12].....	112
Figure 4-14: Data frame .....	114
Figure 4-15: Error frame.....	114
Figure 4-16: Frame description .....	115
Figure 4-17: Important units in the functional architecture.....	117
Figure 4-18: Functional architecture of master node .....	117
Figure 4-19: Graphical representation of the oversampling technique.....	119
Figure 4-20: The FIFO concept .....	120
Figure 4-21: DPR component entity .....	120

Figure 4-22: Graphical representation of the CRC hardware implementation.....	123
Figure 4-23: CRC 15 polynomial division circuit .....	124
Figure 4-24: Functional architecture of the slave nodes.....	125
Figure 4-25: ISensorboard and Main controller communication functional architecture .....	126
Figure 4-26: Transmitter state machine on the ISensorboard.....	128
Figure 4-27: Receiver state machine on ISensorboard.....	130
Figure 4-28: Communication controller state machine on the Main controller .....	132
Figure 4-29: Connection between the power amplifiers and the main controller.....	134
Figure 5-1: Experiment setup .....	141
Figure 5-2: Experimental setup in the laboratory .....	141
Figure 5-3: Receiver waveform analysis (2.24 Mbps) .....	142
Figure 5-4: Transmitter waveform analysis (2.24 Mbps) .....	142
Figure 5-5: Transmitter waveform analysis (8.31 Mbps) .....	143
Figure 5-6: Receiver waveform analysis (8.31 Mbps) .....	143
Figure 5-7: Eye diagram at the receiver end .....	145
Figure 5-8: Eye diagram at the transmitter end.....	145
Figure 5-9: Cross section for jitter and noise measurement [65] .....	146
Figure 5-10: Statistical properties of eye diagram [42] .....	146
Figure 5-11: Eye diagram at the receiver end .....	147
Figure 5-12: Percentage jitter measurement [68] .....	148
Figure 5-13: Eye diagram transmitter end .....	149
Figure 5-14: Noise peak to peak whilst the system was off.....	150
Figure 5-15: Eye diagram of un-terminated transmission lines.....	151
Figure 5-16: UART transmit simulation 1 .....	154
Figure 5-17: UART transmit simulation 2 .....	154
Figure 5-18: Test bench setup.....	155
Figure 5-19: Simulation 1 UART RX .....	156

Figure 5-20: Simulation 2 UART RX .....	156
Figure 5-21: Simulation 3 UART top-level .....	157
Figure 5-22: MATLAB® program calculating the CRC for the 32 bit input message .....	160
Figure 5-23: ModelSim® simulation of the CRC calculation for the 32 bit input message .....	160
Figure 5-24: MATLAB® program calculating the CRC for the 32 bit input message .....	161
Figure 5-25: Modelsim® simulation of the CRC calculation for the 32 bit input message .....	161
Figure 5-26: Test bench setup to verify communication controllers .....	162
Figure 5-27: UART controller ISensorboard verification .....	163
Figure 5-28: UARTcontroller main controller verification.....	164
Figure 5-29: Verifying the FIFO RX component.....	165
Figure 5-30: Verifying the remaining section of the state machine .....	166
Figure 5-31: Error response to loss of synchronization signal.....	167
Figure 5-32: Error response to CRC mismatch .....	168
Figure 5-33: Synchronization verification .....	169
Figure 5-34: Communication timing during normal operation.....	170
Figure 5-35: Communication timing during error conditions. ....	170
Figure 5-36: Eye diagram constructed whilst levitating .....	172
Figure 5-37: 3D representation of the eye diagram whilst the ADES was fully operational .....	173
Figure 5-38: Eye diagram construction and a persistence histogram .....	173
Figure 5-39: Eye diagram constructed as well as vertical persistency histogram .....	174
Figure 5-40: Noise peak to peak (fully operational) .....	177
Figure 5-41: Eye diagram's sampling window.....	178
Figure 5-42: Amplitude separation measured at ringing effect.....	179
Figure 5-43: Overview of internal communication system.....	180
Figure 5-44: Termination of the BLDN cable .....	180
Figure 5-45: Termination of the BLDN cable and the SCSI cable .....	180
Figure 5-46: Framing validation .....	181



Figure 5-47: Data communicated between the ISensorboard and the main controller .....	183
Figure 5-48: Data communicated between power amplifier unit and main controller .....	184
Figure 5-49: Decoded X values .....	185
Figure 5-50: Decoded Y values .....	185
Figure 5-51: Decoded Z values .....	186
Figure 5-52: Decoded error values .....	186
Figure 5-53: Simulation results obtained from sample data 34.....	187
Figure 5-54: Simulation results obtained from sample data 72.....	187
Figure 5-55: Decoded Error frame.....	187
Figure 5-56: Accurate value.....	187
Figure 5-57: Normal operation .....	188
Figure 5-58: Response to loss of sync signal .....	189
Figure 5-59: Command line indicating that the sync error was flagged.....	189
Figure 5-60: Command line indicating that the CRC mismatch error was flagged .....	190
Figure 5-61: Data received from main controller was corrupted.....	190
Figure 5-62: ISensorboard timing during normal operation .....	191
Figure 5-63: Communication timing between the ISensorboard and the main controller.....	192
Figure 5-64: Power amplifier response to the sync signal .....	192
Figure 5-65: Communication timing between the Power amplifiers and the Main controller.....	193
Figure 5-66: Communicated ISensorboard values .....	194
Figure 5-67: Scaled communicated values received from ISensorboard .....	195
Figure 5-68: User interface displaying the position values.....	195
Figure 5-69: Raw unscaled true current values received from power amplifier board 1.....	196
Figure 5-70: Scaled true current values received from power amplifier board 1 .....	197
Figure 5-71: User interface of true current values.....	198
Figure 5-72: Communicated reference value .....	199
Figure 5-73: dSPACE® setup .....	199

Figure 5-74: ADES setup.....	200
Figure 5-75: Position signal of dSPACE®.....	200
Figure 5-76: Position signal of ADES.....	200
Figure 5-77: Sensitivity analysis setup [73].....	201
Figure 5-78: Sensitivity analysis functional breakdown [46].....	202
Figure 5-79: Radial AMB's sensitivity of the X axis.....	203
Figure 5-80: Radial AMB's sensitivity of the Y axis.....	203
Figure C-1-1: UART receiver state machine.....	221
Figure C-1-2: Start bit detection.....	222
Figure C-1-3: WaitFirst counter.....	222
Figure C-1-4: WaitBits counter.....	223
Figure C-1-5: State addition.....	223
Figure C-2-1: FSM for UART transmitter.....	224
Figure C-3-1: State machine implemented on the power amplifier.....	226
Figure C-4-1: State machine implemented on main controller.....	228

## List of tables

Table 2-1: Serial and Parallel data transmission comparison [14] .....	18
Table 2-2: Data transmission topology comparison .....	19
Table 2-3: Differential transmission versus single ended transmission.....	22
Table 2-4: RS 232 standard specifications.....	26
Table 2-5: RS 422 standard specifications.....	26
Table 2-6: RS 485 standard specifications.....	28
Table 2-7: SPI standard specifications.....	30
Table 2-8: USB standard specifications.....	30
Table 2-9: Basic low voltage standard specifications.....	32
Table 2-10: PCI specifications [28].....	33
Table 2-11: Tabulated local bus comparisons [14] .....	34
Table 2-12: Profibus specifications .....	37
Table 2-13: Profibus variants comparison.....	37
Table 3-1: Architecture description.....	55
Table 3-2: Pros and cons of different architectures.....	58
Table 3-3: Deciding factors of architecture selection .....	59
Table 3-4: Refined functional analysis .....	63
Table 3-5: Amount of data to be communicated .....	63
Table 3-6: Data transmission standards.....	65
Table 3-7: Screening 1.....	65
Table 3-8: Screening 2.....	66
Table 3-9: Screening 3.....	66
Table 3-10: Viable communication alternatives.....	66
Table 3-11: RS 485 specifications .....	67
Table 3-12: TIA/EIA 899 specifications [14] .....	68
Table 3-13: USB2 specifications [14].....	69

Table 3-14: IEEE 1284 specifications [14] .....	69
Table 3-15: Fibre optic specifications .....	70
Table 3-16: Decision Criteria .....	71
Table 3-17: Decision matrix .....	72
Table 3-18: Raw score motivation.....	73
Table 3-19: Evaluation matrix .....	75
Table 3-20: Refined functional analysis .....	76
Table 3-21: Amount of data to be communicated .....	77
Table 3-22: Screening 1.....	78
Table 3-23: Screening 2.....	79
Table 3-24: Viable alternatives that satisfy the go/no go constraints .....	79
Table 3-25: Evaluation matrix .....	81
Table 3-26: Raw score motivation.....	82
Table 3-27: Refined functional analysis .....	83
Table 3-28: Amount of data to be communicated .....	84
Table 3-29: Constraints.....	87
Table 3-30: Data to be communicated.....	87
Table 3-31: Amount of data to be communicated .....	88
Table 3-32: SCADA specifications .....	89
Table 3-33: Remote access constraints .....	89
Table 3-34: Fast Ethernet specifications [48] .....	91
Table 3-35: Decision criteria .....	93
Table 3-36: Decision matrix .....	93
Table 3-37: Evaluation matrix .....	94
Table 3-38: Raw score motivation.....	95
Table 4-1: Connector types .....	112
Table 4-2: Transmission parameters .....	118

Table 4-3: XOR truth table .....	123
Table 4-4: Error conditions .....	127
Table 4-5: Error conditions .....	127
Table 4-6: State description of TX process.....	129
Table 4-7: State description of RX process .....	131
Table 4-8: State description of the communication controller situated on the main controller .....	133
Table 4-9: Error conditions .....	135
Table 4-10: Error conditions .....	135
Table 5-1: Key differences between validation and verification testing .....	138
Table 5-2: Physical layer verification .....	139
Table 5-3: Verification test .....	140
Table 5-4: Rise time analysis .....	142
Table 5-5: Rise time analysis .....	143
Table 5-6: Statistical eye diagram measurements on the receiver end.....	148
Table 5-7: Statistical eye diagram measurements on the transmitter end .....	149
Table 5-8: Data link layer verification.....	152
Table 5-9: Transmission parameters specifications.....	153
Table 5-10: Observations concerning the UART TX component .....	155
Table 5-11: Observations concerning the transmission parameters .....	155
Table 5-12: Observations concerning the UART RX component .....	158
Table 5-13: Observations concerning the oversampling procedure .....	158
Table 5-14: Observations concerning the UART top-level.....	158
Table 5-15: Transmission parameters verified.....	159
Table 5-16: Components verified.....	159
Table 5-17: Variables for 32 bit message test.....	160
Table 5-18: Variables for 64 bit message test.....	161
Table 5-19: Results for CRC tests.....	162

Table 5-20: CRC controller specifications.....	162
Table 5-21: Observation concerning the ISensorboard communication controller .....	163
Table 5-22: Observations concerning the main controller's communication controller .....	164
Table 5-23: Observations concerning the loss of the synchronization signal.....	167
Table 5-24: Observations concerning a CRC mismatch .....	168
Table 5-25: ISensorboard and main controller interconnection verification .....	168
Table 5-26: Communication timing & Synchronizations specifications .....	169
Table 5-27: Requirements to validate.....	171
Table 5-28: Statistical properties obtained from horizontal slicing. ....	174
Table 5-29: Statistical properties obtained from vertical slicing .....	175
Table 5-30: Values obtained from random samples .....	186
Table 5-31: Comparing results .....	188
Table 5-32: Sensitivity ratings .....	202
Table 3-1: State description .....	227
Table 4-1: State description .....	229

## List of abbreviations

A/D	Analogue-to-digital converter
ADC	Analogue-to-digital converter
ADES	AMB and drive electronic system
ADSL	Asymmetric digital subscriber line
AMB	Active magnetic bearing
ARCNET	Attached Resource Computer NETWORK
AWG	American wire gauge
B/s	Bytes per second
BER	Bit error ratio
BERT	Bit error rate tester
bps	bits per second
BRAM	Block RAM
B-SPEC	B specification
CAN	Controller area network
CCITT	Consultative committee on international telephone and telegraph
CMOS	Complementary metal-oxide-semiconductor
COTS	Commercial off the shelf
cPCI	Compact PCI
CRC	Cyclic redundancy checks
DAC	Digital-to-analogue converter
DDR	Double data rate
DPR	Dual port RAM
DSP	Digital signal processor
EIA	Electronic industries alliance
EMI	Electromagnetic interference
ESD	Electrostatic discharge
FCS	Frame check sequence
FEC	Forward error correction
FIFO	First in first out
FPGA	Field programmable gate array
FSM	Finite state machine
Gbps	Gigabit per second
GPIB	General purpose interface bus
HD	Hamming distance

A communication sub-system for the ADES

HDL	Hardware description language
I/O	Input/Output
I2C	Inter-integrated circuit
IEEE	Institution of electrical and electronic engineers
IF	Interface
ISDN	Integrated services digital network
ISO	International organization for standardization
LIN-Bus	Local interconnect network
LFSR	Linear feedback shift register
LVDS	Low voltage differential signalling
LVTTL	Low voltage transistor transistor logic
Mbps	millions of bits per second or megabits per second
MBUS	Message-Bus
M-LVDS	Multipoint LVDS
NRZ	Non-return-to-zero
OSI	Open systems interconnect
PC	Personal computer
PCB	Printed circuit board
PCI	Peripheral component interconnect
PCI-X	PCI eXtended
PLB	Processor local bus
PLC	Programmable logic controller
PMC	PCI mezzanine card
PowerPC	Performance optimized with enhanced RISC performance computing
Profibus-DP	Profibus-Decentralized peripherals
Profibus-FMS	Profibus-Fieldbus message specification
Profibus-PA	Profibus-Process automation
R&D	Research and development
RAM	Random access memory
RISC	Reduced instruction set computer
RS	Recommended standard
RTM	Rear transition module
RX	Receive
SBC	Single board computer
SCADA	Supervisory control and data acquisition
SCSI	Small computer system interface



SDRAM	Synchronous dynamic RAM
SERCOS	Serial Real-Time Communication
SMBUS	System management bus
SNR	Signal-to-noise ratio
SPI	Serial peripheral interface
STP	Shielded twisted pair
TEM	Transverse electromagnetic
TIA	Telecommunication industries associations
TX	Transmit
UART	Universal asynchronous receiver/transmitter
UI	Unit interval
USB	Universal serial bus
USS	Universal serial interface
UTP	Unshielded twisted pair
VHDL	VHSIC hardware description language
VHSIC	Very-high-speed integrated circuit
WAP	Wireless application protocol

## List of symbols

$C$	Capacitance
$\eta$	Efficiency
$G$	Conductance
$h$	Height
$I$	Current
$L$	Inductance
$m$	Meter
$R$	Resistance
$\sigma$	Standard deviation
$t$	Time
$\mu$	Mean
$V$	Voltage
$w$	Width

