Synthesis and evaluation of an autonomous neutron monitor system for use in a very low temperature environment

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Supervisor: Prof JEW Holm

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Acknowledgements

“We must always remember with gratitude and admiration the first sailors who steered their vessels through storms and mists, and increased our knowledge of the lands of ice in the South.”

Roald Amundsen

In memory of one of the pioneers in science: Prof Harm Moraal, whose passion for the sciences will always be remembered.

I’d like to thank

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SUMMARY

Synthesis and evaluation of an autonomous neutron monitor system for use in a very low temperature environment

The long standing study field of cosmic rays has been around since 1932 and as such, so has neutron monitors, used to observe these high energy particles.

One of the determining factors influencing the measurement of particles is that of physical location. The higher altitude and latitude monitors were found to observe more particles necessitating a growing scientific need to deploy smaller robust neutron monitors at higher altitude locations closer to both Arctic and Antarctic circles.

Placing an instrument at these types of locations presents a logistical problem for the current mini-neutron monitor design. Lacking the infrastructure to supply power and shelter, such locations were mostly exposed to the elements - exhibiting extremely cold temperature conditions. This required the revaluation of the current monitor designs.

Consequently, from this research a low-power/low-temperature neutron monitor was developed specifically for use in such isolated, harsh low-temperature conditions.

Using Design Science Research (DSR) as the primary research methodology, the process of synthesis was combined with research to deliver both a real-world solution along with a knowledge base contribution in the form of meta-artefacts.

The research problem of extreme environment operation was addressed by the study of low-temperature components. Failure mechanisms were limited by appropriate selection of specialized low-temperature components. To provide extra protection, an insulated heated enclosure was modelled to provide the system with additional safeguards against the extreme operating conditions.

The problem of remote data acquisition was addressed by an autonomous design. A unit was built capable of storing data locally and responding to environmental influences without the need for human intervention. The unit was also made to regulate the use of energy, thereby controlling its enclosed temperature.

Although this research focused on the development of a complete neutron monitor system, the physical solution was limited to the electronic capturing unit and a theoretical mechanical enclosure. The enclosure design was focused on an environmentally-sealed easily-transportable unit. As validation of model and construct, all the supporting mathematical models and experimental testing are presented in this research.

Keywords: Neutron monitor, Design Science Research, low-power design, low-temperature design and battery operated data acquisition system.
OPSOMMING

**Sintese en evaluering van ’n autonome neutron monitor sisteem, vir gebruik in ’n baie lae temperatuur omgewing**

Die studieveld van kosmiese strale is al lank in bestaan (sedert 1932) en daarom ook die gebruik van neutron monitors om hierdie hoë energie deeltjies waar te neem.

Een van die bepalende faktore vir die meet van dié deeltjies is die fisiese ligging van die monitor. ’n Fisiese hoër monitor, geplaas by ’n hoër breedtegraad, is gevind om meer deeltjies te meet. Dus is daar ’n groeiende behoefte om kleiner, meer geharde neutron monitors op beide Arktiese- en Antarktiese-liggings te plaas.

Deur instrumentasie op hierdie liggings te plaas het bydraende logistieke vereistes teweeggebring waaraan die huidige mini-neutron monitors nie voldoen het nie. Hierdie liggings het ’n gebrek aan infrastruktuur wat nie krag of afskerming vir die monitor bied nie en dus die bloedstel aan uiterste koue. Dus was daar die vereiste om die huidige monitor te herontwerp en as gevolg daarvan, is daar navorsing gedoen in die ontwerp van ’n lae-temperatuur elektroniese toestel vir die gebruik in geisoleerde lae-temperatuur omgewings.

“Design Science Research” (DSR) is gebruik as die primêre navorsingsmetodiek. Deur die proses van sintese te kombineer met navorsing, is daar beide ’n regte-wêreld oplossing en kennis as produk gelewer.

Die ekstreme omgewing navorsingsprobleem is deur ’n studie van lae-temperatuur komponente benader. Mislukkingsmeganismes is beperk deur spesifieke lae-temperatuur komponentkeuses te maak. Om ekstra afskerming te bied teen die omgewing, is ’n verhitte en geïnsuleerde omhulsel ontwerp en gemoduleer.

Autonome ontwerp is gebruik om ’n veldinstrument te maak wat in staat is om data intern te berg en ook besluite te maak aangaande die omgewingsinvloede - dit alles sonder menslike ingryping. Die ontwerp was ook so gemaak om energiegebruik te beheer deur die omhulsel se interne temperatuur te reguleer. Alhoewel die navorsing fokus op die ontwerp van ’n volledige neutron monitor, is die ontwikkeling beperk tot ’n elektroniese toestel en die meganiese omhulsel is as ’n teoretiese model aangebied. Die omhulsel-ontwerp het gefokus op omgewingsafskeuring en vervoerbaarheid.

Om beide die elektroniese produk en die teoretiese ontwerp te regverdig, word al die ondersteunde wiskundige modelle en experimente in dié navorsingsdokument gelewer.

**Sleutelwoorde:** Neutron monitor, ontwerpnavorsing, lae-energie ontwerp, lae-temperatuur ontwerp en batterygedrewen instrumentasie.
<table>
<thead>
<tr>
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<th>Definition</th>
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<tr>
<td>AC</td>
<td>Alternating current</td>
</tr>
<tr>
<td>ADC</td>
<td>Analog to digital converter</td>
</tr>
<tr>
<td>ARM</td>
<td>Advanced RISC machine</td>
</tr>
<tr>
<td>BJT</td>
<td>Bipolar junction transistors</td>
</tr>
<tr>
<td>CAD</td>
<td>Computer-aided design</td>
</tr>
<tr>
<td>CISC</td>
<td>Complex instruction set computing</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary-symmetry metal–oxide–semiconductor</td>
</tr>
<tr>
<td>CSR</td>
<td>Centre for space research</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital to analogue converter</td>
</tr>
<tr>
<td>DAS</td>
<td>Data acquisition system</td>
</tr>
<tr>
<td>DC</td>
<td>Direct current</td>
</tr>
<tr>
<td>DR</td>
<td>Design research</td>
</tr>
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<td>DSR</td>
<td>Design science research</td>
</tr>
<tr>
<td>EDM</td>
<td>Engineering development model</td>
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<tr>
<td>EMC</td>
<td>Electromagnetic conductivity</td>
</tr>
<tr>
<td>EMI</td>
<td>Electromagnetic interference</td>
</tr>
<tr>
<td>FET</td>
<td>Field effect transistors</td>
</tr>
<tr>
<td>FU</td>
<td>Functional unit</td>
</tr>
<tr>
<td>GPS</td>
<td>Global positioning system</td>
</tr>
<tr>
<td>GNSS</td>
<td>Global navigation satellite system</td>
</tr>
<tr>
<td>IGY</td>
<td>International geophysical year</td>
</tr>
<tr>
<td>IP</td>
<td>Ingress protection</td>
</tr>
<tr>
<td>I2C</td>
<td>Inter integrated circuit</td>
</tr>
<tr>
<td>LPT-NM</td>
<td>Low-power/low-temperature neutron monitor</td>
</tr>
<tr>
<td>MCDM</td>
<td>Multi-criteria decision-making</td>
</tr>
<tr>
<td>MCU</td>
<td>Micro-control unit</td>
</tr>
<tr>
<td>MIPS</td>
<td>Million instructions per second</td>
</tr>
<tr>
<td>MLC</td>
<td>Multi-level cell</td>
</tr>
<tr>
<td>MMC/SD</td>
<td>Multimedia card / Secure digital</td>
</tr>
<tr>
<td>MPU</td>
<td>Microprocessor unit</td>
</tr>
<tr>
<td>NM</td>
<td>Neutron Monitor</td>
</tr>
<tr>
<td>MNM</td>
<td>Mini-neutron monitor</td>
</tr>
<tr>
<td>MNM-DAS</td>
<td>Mini-neutron monitor data acquisition system</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>PV</td>
<td>Photovoltaic</td>
</tr>
<tr>
<td>SANAES</td>
<td>South African national Antarctic expedition</td>
</tr>
<tr>
<td>SLC</td>
<td>Single-level cell</td>
</tr>
<tr>
<td>SPI</td>
<td>Serial peripheral interface</td>
</tr>
<tr>
<td>UART</td>
<td>Universal asynchronous receiver/transmitter</td>
</tr>
<tr>
<td>USB</td>
<td>Universal serial bus</td>
</tr>
<tr>
<td>RISC</td>
<td>Reduced instruction set computing</td>
</tr>
<tr>
<td>RTCC</td>
<td>Real-time clock and calendar</td>
</tr>
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<td>TLC</td>
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1 Introduction to cosmic rays and neutron monitors

The purpose of this study is to synthesise and evaluate the electronic subsystem of a mini neutron monitor (MNM) as a stand-alone acquisition instrument with an internal power source inside a low temperature environment with temperatures down to –60 °C.

It is the intention in the cosmic-ray community that MNMs should replace an existing network of around 40 neutron monitors (NMs) around the world. This network is more than 50 years old and expensive to operate and maintain. Previous studies by Fuchs and Kruger [1] [2] have described a miniature version of these instruments. The drawback of these MNMs is that their counting rate is ten times lower than that of standard NMs. This can be addressed by placing MNMs at high latitudes because, as will be shown in Section 1.2, the counting rate of these instruments increases significantly with increased altitude, such as on mountains. For example, at 3 000 m an MNM counts as much as a standard NM at sea level.

Many of these planned MNMs can be placed in existing mountain infrastructures such as mountain huts, meteorological stations, cable-car stations and high-altitude science experiments such as optical telescopes. Some of these high-altitude stations, however, are no more than simple enclosures. They do not have continuous power and are often visited only once a year in summer.

Therefore: Develop the Kruger/Fuchs design [1] [2], with such low power requirements that it can last up to one year and operate at ~ -60 °C.

1.1 Cosmic-rays defined

Cosmic rays are high-energy particles, i.e. particles with energies in excess of MeV\(^1\). These particles originate from outside the heliosphere of our solar system and are generally caused by galactic events. The propagation of these particles is dependent on the time-varying magnetic field of the solar wind.

Cosmic rays can also be categorised into two groups, both high-energy and low-energy particles. High energy (>20 GeV) cosmic rays originate from our own galaxy called “galactic cosmic rays” (GCR). The low energies cosmic rays (<50 MeV) are associated with the occasional impulsive bursts generated near the sun, called solar cosmic rays (SCR), and are considered “anomalous cosmic radiation”, which is accelerated within the heliosphere of the Solar System [2].

\(^1\) Electron Volt, a measure of potential energy
1.2 Cosmic-rays in the magnetosphere

Cosmic rays are influenced by the heliosphere; it stands to reason that the same effect would be visible within the magnetosphere of the earth. In 1932 Clay and Berlage \[3\] demonstrated a latitudinal effect in which the intensity of cosmic rays increased with geomagnetic latitude. This happens because the magnetic field increases inversely with latitude; charged particles are therefore deflected by an increase in the geomagnetic magnetic field. To describe this effect a parameter called cut-off rigidity, $R_C$, is defined. This describes the minimum momentum per unit charge that a particle requires to reach a certain geographical location \[3\].

One of the long-term goals of cosmic ray research has been the accurate characterisation of particle trajectories. In the mid-1960s these trajectories were considered so difficult to calculate that only partial grids were published. It was only in 1966 that Shea and Smart \[4\] produced a partial grid covering specific areas of the world, and only by 1968 that they published a complete grid using the Epoch 1955 geomagnetic field model. The model had a resolution of 36 (5° per latitude) by 24 (15° per longitude) grid points. Further studies validated the use of the geomagnetic field model, but required the decadal update of geomagnetic field model values \[4\]. Shown in Figure 1-1 is the vertical cut-off rigidity as calculated from the Epoch 2000 geomagnetic field model data.

![Figure 1-1 Cut-off rigidity in terms of GeV, based on Epoch 2000 data [5]](image)

This vertical cut-off rigidity model can be used as a good first approximation for non-directional cosmic ray detections. This means that NMs placed at the poles would detect particles with rigidities higher than 0 GeV whilst NMs placed near the equator in East Asia would only detect particles with rigidities higher than ~17 GeV. Consequently, detectors at the Poles show the largest variations due to solar activity.
1.3 Cosmic-rays in the atmosphere

1.3.1 Atmospheric path

The second factor that influences the measurements of cosmic rays is that of the atmospheric depth. Cosmic rays, consisting mostly of protons which reach and collide with the atmosphere, are called “primary cosmic rays” [2]. These primary cosmic rays interact with the nuclei in the upper atmosphere producing secondary particles of neutrons and protons, as illustrated in Figure 1-2 below.

Secondary cosmic rays similarly interact with the atmospheric molecules producing added secondary particles, cascading in what is called an “air shower”. The composition of the secondary particles is grouped into the following three types:

- Protons (p) and neutrons (n) (nucleonic component);
- Electrons (e⁻), positrons (e⁺) and gamma rays (γ) (electromagnetic / soft component);
- Muons (π⁺) (hard component).

This cascading effect which happens in the uppermost 10% of the atmosphere continues down until the particles lack the required energy to create further secondary particles. From that point on no further secondary particles are created and the particle density attenuates with each atmospheric particle collision. Of the three types of particles created, cosmic ray studies with NMs primarily measure the nucleonic [2].

![Figure 1-2 Air shower [2]](image-url)
1.3.2 Atmospheric attenuation

Since secondary cosmic rays are attenuated in the lower 90% of the atmosphere, not all secondary particles reach the earth’s surface. Therefore, the intensity of cosmic rays is a function of atmospheric pressure. The change in counting rate $N$, is shown to be:

$$N = N_0 e^{\alpha(P_0 - P)}, \quad (1-1)$$

where $\alpha$ = barometric coefficient, $P_0$ = reference barometric pressure (mBar), $P$ = barometric pressure at the counter, and $N_0$ = reference counting rate at $P_0$.

The barometric pressure $P$ at an altitude $h$, can be shown to be:

$$P \approx P_0 e^{-0.00012h}, \quad (1-2)$$

where $P_0$= standard atmospheric pressure at sea level with a temperature of 20 °C (293.15 K).

Substituting the U.S. Sea Level Standard Atmospheric value of 1 013.25 mBar and a typical barometric coefficient of $\alpha = -0.007$ mBar into equation (1-1) yields the intensity vs. height profile shown in Figure 1-3.

![Figure 1-3 Count rate of a monitor vs. height above sea level](image)

From this figure it can be seen that at an altitude of 3 300 m, the counting rate of a detector increases by ten times and by up to 100 times at 8 700 m. Any MNM deployed at one of many 3 000 m sites is thus the equivalent of a 5-NM64 at sea level. Making it possible to deploy a MNM at many 3 000 m sites as the equivalent to a 5-NM64 at sea level [1].

1.4 Particle and radiation counters

Section 1.3 showed that primary cosmic rays are transformed into secondary cosmic ray particles and therefore the measurements of these secondary particles are the indirect means to
study the intensity of cosmic rays. As shown in G. Knoll, Radiation Detection and Measurement [6], the following sections describe the gas-filled particle detectors used in cosmic ray neutron monitors.

1.4.1 Particle detection

High-energy particles cannot be measured directly, but rather through the interaction thereof with other atoms and molecules. These interactions produce both excited and ionized molecules, which are shown in the chemical equation [6]:

\[ X + p^1 \rightarrow X^+ + e^- + Q, \]  \hspace{1cm} (1-3)

where \( p^1 \) = sub-atomic particle,
\( X \) = molecule,
\( X^+ \) = ionized molecule,
\( e^- \) = electron, and
\( Q \) = kinetic energy produced by the reaction.

The combined ionized molecule and electron is called an ion pair, having opposite charges. The original sub-atomic particle also has to have sufficient energy to ionize the molecule and if the particle has adequate energy, a collision can cause multiple ionization events.

1.4.2 Ion chamber

The simplest charged particle detector is an ion chamber, as shown by Figure 1-4. As the charged particle travels through the detector gas, a trail of ion pairs is left along its trajectory. The detection of an ion pair is accomplished by means of an electrical field created by applying a high voltage across a parallel plate interface.

The electrical field allows detection by separating and preventing the recombination of the ion pairs. Separation is achieved by drawing the individual units of the ion pair towards the electrodes: the positive ion towards the cathode and the electron towards the anode. As the ions are drawn into the electrodes they recombine and current is created.

![Figure 1-4 Ion chamber [6]](image-url)
The excitation particle $p^1$ passes through a gas medium and ionizes molecules with each collision, creating charged ion pairs which are drawn to the electrode plates. With recombination, current is produced moving through the high-voltage circuit. The current measured is proportional to the total amount of charge from each ion pair, therefore proportional to the energy of the original exciting particle.

### 1.4.3 Proportional counter

The sensitivity of the ion chamber is proportional to the electric field responsible for the drift towards the electrodes. An increased electrical field will produce an increased energy in each pair. For this reason, the geometry of the anode becomes important.

**Figure 1-5 Simple electric field geometry**

In a simple illustration, the field lines shown for a parallel plate are uniform throughout an electrode separation, whereas with a cylindrical geometry, the field lines are focused into a tightly concentrated focal point. It is for this reason that the electrical field of a single wire within a cylinder is used to increase the energy of the electron. The electrical field $E$, at a radial distance $r$, is shown to be:

$$E(r) = \frac{V}{r \ln(b/a)}, \quad (1-4)$$

where $V$ = applied voltage,
$\ a$ = anode radius, and
$\ b$ = cathode radius.

Substituting arbitrary values produces Figure 1-6:
At a certain critical point the ion pair will acquire sufficient energy to start stripping electrons from surrounding atoms, called “Townsend discharge”. This, “the avalanche region”, is shown in Figure 1-7.

As in the ion chamber, an energetic particle may produce a single or multiple ion pairs depending on the original energy available. Each liberated electron is drawn towards the anode, accelerating within the electrical field. They gain so much energy that they are able to ionize more particles, cascading towards the electrode. This process is called “gas multiplication”. The amount of current produced from a single Townsend discharge is therefore proportional to the number of cascading events. The result of the gas multiplication is to allow the amplification of the original ion pair charge.

The multiplication factor $M$ can be calculated using the equation [6]:

$$\ln M = \frac{V}{\ln(b/a)} \cdot \ln\left(\frac{2}{\Delta V}\right) \left(\ln\left(\frac{V}{p \times a} \times \ln(b/a)\right) - \ln K\right),$$

where $K = \text{minimum value of } E/p \text{ below which multiplication cannot occur, and } p = \text{gas pressure}.$ As before: $V = \text{applied voltage},$
\( a \) = anode radius, and  
\( b \) = cathode radius.

Consequently, the charge \( Q \) of the original ionization event \( n_0 \) is:

\[
Q = n_0 e M, \tag{1-6}
\]

where \( e \) = charge of an electron, and  
\( M \) = multiplication factor.

In conclusion, the current obtained from such a proportional counter is proportional to the energy of the original ionizing particle.

### 1.4.4 Geiger mode

In Geiger mode the Townsend discharge is still in effect, however the electric field contributes so much energy to the electron, that it starts producing UV photons. These UV photons, also capable of liberating electrons, move laterally to the axis of the anode and consequently lead to an additional series of avalanches called a Geiger discharge. Each avalanche produces more electrons and UV photons, which leads to further avalanches enveloping the anode. Figure 1-8 shows the production of avalanches caused by the release of UV photons.

As a result, a single ionisation event will cause large portions of the anode to saturate with ion pairs of which the ionisation charge is independent of the original ionizing event.

Once the Geiger discharge reaches a certain size, the avalanches start affecting one another in such a way that all of the avalanches are terminated. Therefore, in Geiger mode the amount of avalanches remains relatively fixed; making measured pulses the same amplitude. As a result Geiger counters have the same amplitude for each pulse, irrespective of the energies of the radiation particles [7]. The pulses become a function of geometry and field strength, losing all spectral information.
Introduction to cosmic rays and neutron monitors

Chapter 1

School of Electrical, Electronic and Computer Engineering
North-West University

1.5 Neutron physics

Secondary cosmic ray neutrons reaching the earth’s surface may still have energy in the range of 500 KeV to 100 MeV and therefore are considered fast neutrons.
Neutrons carry no charge and consequently they cannot interact with matter by means of Coulomb forces, making their detection possible only through nuclear reactions. These reactions result in charged energetic particles, such as protons \((n, p)\) and alpha particles \((n, \alpha)\).

However the energy of a fast neutron is such that it may pass through material without interacting with its atoms. To measure this collision/reaction probability, a value called the cross section is used, measured in units of barns \(\left(10^{-28} \text{ m}^2\right)\).

Figure 1-11 shows the cross section for three common neutron nuclear reactions:

![Figure 1-11 Cross section versus neutron energy][1]

The cross section is inversely proportional to the kinetic energy and therefore decreases as the neutron’s kinetic energy increases. It is thus more likely that a thermal neutron of 0.025 eV, rather than a high-energy neutron, will trigger a nuclear reaction. For this reason, the proportional limit for the detection of neutrons is limited to neutrons with energies below that of 0.5 eV [6]. Thus, to detect a fast neutron, modified schemes have to be used to decelerate the neutron to thermal energies.

1.5.1 Moderators and reflectors

To reduce the neutron’s energy, the particle has to be slowed down; and to increase the neutron detection probability adequately it has to be slowed to the energy level of that of a thermal neutron. This process of reduction is called thermalisation or moderation [2].

A moderator makes use of elastic scattering to achieve thermalisation. This is the collision of a neutron with another atom’s nucleus. This collision is elastic and does not result in a nuclear reaction. Fast neutrons undergo scattering once they move through condensed matter as the
result of kinetic energy transferring between the neutrons and other atoms. With each collision the neutron slows down, to the point where thermal equilibrium is reached [2].

Materials with lighter nuclei absorb more energy per collision and therefore have a more prominent thermalisation effect. For that reason hydrogen, with its small nucleus, is a preferred moderator. With a hydrogen nucleus, a neutron can lose up to all of its energy in a single collision [2].

Common moderator materials such as paraffin wax, polyethylene (CH₂) and water (H₂O) are rich in hydrogen. The average thickness of a paraffin moderator is 3.7 cm, or 2.0 cm for a polyethylene moderator. The problem with detecting thermal neutrons from cosmic ray events is that in any environment background thermal neutrons are present, subsequently mixing in with thermalized neutrons. Thus the detector not only detects cosmic rays, but also background thermal neutrons.

Therefore the secondary function of a moderator is to reflect or absorb background thermal neutrons as background thermal neutron would lack the energy to pass through the dense moderator material.

Figure 1-12 shows the thermalisation of fast neutrons and the deflection of thermal neutrons, allowing only fast neutrons to reach the detector inside.

![Moderator / reflector](image)

**Figure 1-12** Moderator / reflector [6]

### 1.5.2 Producer

To enhance the sensitivity of a neutron counter, a producer is used that creates several neutrons for each arriving event. Such a producer makes use of neutron emissions resulting from the spallation of the nucleus of a heavy atom such as lead. The shattering nucleus ejects protons and neutrons, each absorbing a fraction of the kinetic energy. Concurrently the remaining nucleus is excited to a higher energy and starts emitting low energy neutrons and protons in an attempt to release the excited energy; this de-excitation process is called evaporation. The
evaporated neutrons therefore have a lower energy than the original neutron and may lead to additional spallation events. The result is multiple low-energy neutrons.

Lead (Pb) is a common producer material and can produce up to ten evaporation neutrons for an incident neutron. As a result the detector sensitivity can be multiplied by around ten times [8]. This does, however, lead to the possibility that a single incoming neutron may lead to the detection of multiple events. This effect is called multiplicity.

1.5.3 Common neutron nuclear reactions

Neutron monitors consist of either boron-tri-fluoride ($^{10}$BF$_3$) or Helium 3 ($^3$He) proportional counters. [7] [8].

The mean sensitivity of a $^3$He reaction is proportional to the cross section of a thermal neutron of 5 330 barns. Once a successful reaction, as shown by equation (1-7), occurs, two charged hydrogen isotopes H$^1$ and H$^3$ are produced along with an excitation energy Q = 764 KeV.

$$^3\text{He} + n^1(\text{thermal}) \rightarrow \text{H}^1 + \text{H}^3 + Q$$  

(1-7)

The second type of reaction shown by (1-8) uses BF$_3$ gas with thermal cross section of 3840 barns, thus with a sensitivity 1.4 times less than that of $^3$He.

$$\text{B}^{10} + n^1(\text{thermal}) \rightarrow \text{Li}^7 + \text{H}_e^4 + Q$$  

(1-8)

Although the reaction sensitivity is less, the reaction produces 2.79 MeV of energy, therefore making the pulse potentially 3.6 times larger than that of the $^3$He reaction.

1.6 Neutron detector

From the previous discussion, a complete view of a fast neutron / cosmic ray detector can now be shown.

![Figure 1-13 Ionization of BF$_3$ gas inside the neutron detector](image)

The neutron counter can be divided into five functional components:
Chapter 1

Introduction to cosmic rays and neutron monitors

- **Reflector:**
  The function of the reflector is to shield the detector against background thermal neutrons, making sure only higher energy neutrons are allowed to propagate through the counter.

- **Producer:**
  From the producer two functions are achieved: multiple neutrons (up to ten times the original) are evaporated and the energy is divided amongst the new produced neutrons.

- **Moderator:**
  Incoming neutrons are thermalized down to 0.025 eV, allowing detection by the counter.

- **Ionizing Gas:**
  The counter gas produces a nuclear reaction from the original thermal neutron.

- **Proportional Counter**
  In the proportional counter region the ion pair electrons are attracted towards the anode and multiplied by means of the Townsend discharge effect. When they are finally recombined, they cause the flow of current proportional to the original cosmic ray particle event energy.

### 1.7 Neutron monitor layout

The basis of a neutron monitor is described by the following configuration:

![Proportional mode](image)

**Figure 1-14 Basic neutron monitor operational units**

For the purpose of cosmic ray detection, a neutron monitor is set up as a proportional counter. This requires a gas-filled chamber, as mentioned in Section 1.4.3, with an electrical field set up within the chamber using a stable high voltage source.
Thereafter pulses are observed as small current discharges. These current discharges are converted to voltage pulses in the order of 1 mV. This requires an amplification stage to amplify the pulses to an adequate value.

Thereafter, using a predefined threshold value, a discriminator is used to eliminate small pulses due to electronic noise. When pulses larger than the threshold value are detected, a counter circuit is initialized, logging the pulse event.

### 1.8 Pulse discrimination

With each neutron event, a significant amount of energy is deposited within the filling gas, which produces a signal pulse. Because of gas multiplication, the energy varies with the voltage applied to the detector. This is known as the "counting curve", as shown in Figure 1-10. Therefore, the appropriate operating voltage is chosen by application, in this case “proportional mode”. Within this proportional mode, the amplitude of each individual pulse carries information regarding the energy of the charged particle.

![Figure 1-15 Example of pulse shape](image)

Taking into account that the system is not without noise, a threshold value must be chosen above the noise level of the system. For that reason, the pulse height spectra of the system must be assessed. Pulse height spectra involve the measurement of the statistical occurrence of each pulse height, as shown by Figure 1-16.
To generate the pulse height spectra, pulses of equal height are grouped. As shown in Figure 2-16 the number of pulses within the measured heights H1 and H2 would represent a binned group. Where H5 shows the maximum pulse height, H4 indicates amplitudes about where most pulses will be found and H3 the amplitude value where relatively few pulses will occur. Additionally all pulses lower than H3 are considered to be noise-related spurious pulses.

In setting up a pulse counting measurement, it is desirable to establish an operating point that will provide maximum stability over long periods of time. For that reason the ideal discriminator value would be H3, counting the least noise and the maximum valid number of pulses.

### 1.9 Neutron monitors

An Austrian physicist, Victor Hess, observed cosmic rays for the first time in 1912, whilst performing a balloon flight with two ionization chambers. From around 1950, scientists have been studying and observing these high-energy particles by means of neutron monitors [9]. The first neutron monitor was installed by J.A. Simpson at the University of Chicago in 1951 [10]. By 1957/8 Simpson had modified the monitor for use during the International Geophysical Year (IGY). It consisted of 12 × 10BF₃ counters. Thereafter H. Carmichael [2] designed the NM64 10BF₃ super neutron monitor in 1964. In 1964 Hatton and Carmichael, using large Chalk River 10BF₃ proportional counters, studied the NM64 monitors design in detail. This resulted in an improved counting rate per unit area for both the IGY and NM64 monitors. Respectively, the efficiency of the IGY was improved from 1.9 % to 5.7% and the NM64 monitor improved by 3.3 times [11]. Table 1-1 and Table 1-2 give a detailed exposition of the currently existing NM configurations.
Table 1-1 Comparison between IGY and NM64 neutron monitors

<table>
<thead>
<tr>
<th>Type of Counter</th>
<th>NM-64</th>
<th>Standard IGY</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>BP-28 / LND25373</td>
<td>NW G15-35A</td>
</tr>
<tr>
<td>Number of Counters</td>
<td>6</td>
<td>12</td>
</tr>
<tr>
<td>Counter Spacing</td>
<td>50</td>
<td>15.25</td>
</tr>
<tr>
<td>Moderator Material</td>
<td>Low Density Polyethylene</td>
<td>Paraffin</td>
</tr>
<tr>
<td>Average Moderator Thickness (cm²)</td>
<td>1.84</td>
<td>2.95</td>
</tr>
<tr>
<td>Producer Material</td>
<td>Lead</td>
<td>Lead</td>
</tr>
<tr>
<td>Average Producer Thickness (cm²)</td>
<td>156</td>
<td>153</td>
</tr>
<tr>
<td>Projected Top Area of Producer (cm²)</td>
<td>$6.21 \times 10^4$</td>
<td>$1.9 \times 10^4$</td>
</tr>
<tr>
<td>Reflector Material</td>
<td>Low Density Polyethylene</td>
<td>Paraffin</td>
</tr>
<tr>
<td>Average Reflector Thickness</td>
<td>7.0</td>
<td>25.8</td>
</tr>
</tbody>
</table>

Table 1-2 Types of counter [12]

<table>
<thead>
<tr>
<th></th>
<th>BP-28</th>
<th>LND25373</th>
<th>NW G15-35A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gas Type</td>
<td>BF₃</td>
<td>BF₃</td>
<td>96 % $^{10}$B</td>
</tr>
<tr>
<td></td>
<td>96 % $^{10}$B</td>
<td>97 % $^{3}$He + 3 % CO₂</td>
<td>96 % $^{10}$B</td>
</tr>
<tr>
<td>Effective Diameter</td>
<td>14.8 cm</td>
<td>4.8 cm</td>
<td>3.8 cm</td>
</tr>
<tr>
<td>Effective length</td>
<td>191 cm</td>
<td>191 cm</td>
<td>87 cm</td>
</tr>
<tr>
<td>Pressure (mm-Hg)</td>
<td>200</td>
<td>3040</td>
<td>450</td>
</tr>
<tr>
<td>Thermal Neutron</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Absorption Path Length</td>
<td>41.0 cm</td>
<td>1.9 cm</td>
<td>18.2 cm</td>
</tr>
</tbody>
</table>

Approximately 100 of these NMs have been built since 1957 [13]. The Centre for Space Research (CSR) at the North-West University (NWU) operates four such NMs: the Tsumeb, Potchefstroom, Hermanus and SANAE NMs.

1.9.1 Tsumeb neutron monitor

Figure 1-17 Tsumeb, Namibia, since July 1976

The Tsumeb monitor, situated 12 kilometres north-west of the Namibian town Tsumeb, was established by the Max Planck Society in December 1976 [10]. This monitor consists of 18 NM64 counters, measuring an average of 1 220 000 counts per hour at a cut-off rigidity of 9.2 GeV and an atmospheric depth of 879 mBar.
1.9.2 Potchefstroom neutron monitor

![Potchefstroom, South Africa, since May 1971](image)

The Potchefstroom NM is a 15 counter IGY-type NM. This monitor measures about 213 000 counts per hour at a cut-off rigidity of 7.2 GeV and an atmospheric depth of 869 mBar.

1.9.3 Hermanus neutron monitor

![Hermanus, South Africa, since July 1957](image)

The Hermanus monitor has been operating since July 1957 and is situated within the Hermanus Magnetic Observatory, currently the site of SANSA Space Science. It consists of a 12 NM64 Chalk River neutron counter, measuring about 453 500 counts per hour at a cut-off rigidity of 4.9 GeV and an atmospheric depth of 1 013 mBar.
1.9.4 SANAE neutron monitor

![SANAE, Antarctica, since April 1997](image)

The latest NM, the SANAE IV (Antarctica) monitor, has been operating since April 1997, although the project has been running since January 1964, moving with the relocation of the SANAE base. The SANAE IV NM consists of a 6 NM64 monitor and a 4 NMD (neutron moderated detector) monitor. The SANAE NMs are operated in a snow environment and are therefore raised as high as possible from the snow level. They are located on the upper floor of the SANAE station, reducing the effect of externally produced neutrons. The 6 NM64 monitor measures approximately 627 000 counts per hour, and the 4 NMD monitor, 32 800 counts per hour, both at a cut off rigidity of 0.75 GeV and an atmospheric depth of 879 mBar.

![CSR monitor normalized monthly counting rates](image)

**Figure 1-21 CSR monitor normalized monthly counting rates [16]**

Figure 1-21 shows the comparison of the four CSR monitors in terms of the normalized (up to 100 for March 1987) counting rates. Because each monitor differs in efficiency, counting rates must be normalised to compare data effectively.

These four NMs provide data at various latitudes or cut-off rigidities, which is important for the study of time-varying heliospheric magnetic influences on cosmic rays [2].
1.9.5 Relevance of the upgrade and expansion of the monitor network

Of the current global network of NMs, less than half of the stations are still in use. Outdated electronics and financial constraints have led to the further deterioration of the remaining monitors, some of which have been operating for at least 60 years. Failing and outdated hardware has led to the need for a strategy and development plan for the upgrade and replacement of these obsolete monitors [2].

For this reason the CSR initiated a programme to renew and update electronics of existing NMs over the last 10 years. It also embarked on the development of a calibration NM (CNM) [2], which developed into a MNM [1].

1.10 Potential locations

With the proposed new NM, locations are therefore needed to operate this monitor at sufficient counting rates. The list of the existing monitor network was used to select possible future locations for the MNM. The list was also divided into a world map of existing monitors and the Antarctic bases that may potentially house future monitors. The global NMs were limited to NMs above 2 000 m sea level.

Table 1-3 Existing monitors [13] [4]

<table>
<thead>
<tr>
<th>Base Name</th>
<th>Altitude</th>
<th>Type</th>
<th>Rigidity</th>
<th>Counting Factor from Altitude</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Haleakala</td>
<td>3 052</td>
<td>18NM</td>
<td>12.91</td>
<td>8.53</td>
<td>20.72° N 156.6° W</td>
</tr>
<tr>
<td>Climax</td>
<td>3 400</td>
<td>12IGY</td>
<td>2.99</td>
<td>10.76</td>
<td>39.37° N 106.18° W</td>
</tr>
<tr>
<td>Mexico</td>
<td>2 274</td>
<td>6NM</td>
<td>8.60</td>
<td>5.185</td>
<td>19.33° N 99.18° W</td>
</tr>
<tr>
<td>Huancayo</td>
<td>3 400</td>
<td>12IGY</td>
<td>12.92</td>
<td>10.76</td>
<td>02.03° S 77.33° W</td>
</tr>
<tr>
<td>Jungfraujoch 1</td>
<td>3 475</td>
<td>12IGY</td>
<td>4.61</td>
<td>10.76</td>
<td>46.55° N 07.98° E</td>
</tr>
<tr>
<td>Lomnicky’ S’tit</td>
<td>2 634</td>
<td>8NM</td>
<td>3.98</td>
<td>6.69</td>
<td>49.20° N 20.22° E</td>
</tr>
<tr>
<td>Alma Ata</td>
<td>3 340</td>
<td>18NM</td>
<td>6.61</td>
<td>10.17</td>
<td>43.25° N 76.92° E</td>
</tr>
<tr>
<td>Mt-Norikura</td>
<td>2 770</td>
<td>12NM</td>
<td>11.48</td>
<td>7.12</td>
<td>36.11° N 137.55° E</td>
</tr>
</tbody>
</table>
Figure 1-22 Potential locations with high altitudes [13] [4]

The second list is Antarctic bases above 2 000 m. At that altitude, it can be seen that the cut-off rigidity for most of these locations is close to zero.

Table 1-4 Antarctic bases above 2 000 m

<table>
<thead>
<tr>
<th>Base Name</th>
<th>Altitude</th>
<th>Rigidity</th>
<th>Counting Factor from Altitude</th>
<th>Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Amundsen-Scott</td>
<td>2830 m</td>
<td>0</td>
<td>7.57</td>
<td>89.99° S 139.27° E</td>
</tr>
<tr>
<td>Concordia Dome C</td>
<td>3220 m</td>
<td>0</td>
<td>9.60</td>
<td>75.10° S 123.39° E</td>
</tr>
<tr>
<td>D85 ski way</td>
<td>2850 m</td>
<td>0</td>
<td>7.57</td>
<td>74.15° S 134.15° E</td>
</tr>
<tr>
<td>Dome Fuji</td>
<td>3810 m</td>
<td>0.06</td>
<td>13.43</td>
<td>77.32° S 039.70° E</td>
</tr>
<tr>
<td>Kohnen</td>
<td>2900 m</td>
<td>0.24</td>
<td>8.04</td>
<td>75.00° S 000.07° E</td>
</tr>
<tr>
<td>Mid-Point</td>
<td>2520 m</td>
<td>0</td>
<td>6.29</td>
<td>75.54° S 145.82° E</td>
</tr>
<tr>
<td>Vostok</td>
<td>3500 m</td>
<td>0.8</td>
<td>11.39</td>
<td>72.00° S 002.53° E</td>
</tr>
</tbody>
</table>
Antarctica has some of the coldest winters ever recorded, making these locations extremely hazardous for equipment.

*Therefore, the purpose of this work is to improve the existing NM so that it can operate at temperatures as low as -60 °C. Furthermore, since many of the Antarctic bases are unattended in winter, this MNM has to function on an energy supply that can last a full year.*
2 Design methodology

This research requires the creation of a new neutron monitor system. Thus, a methodology is needed to address two points of interest: “Design theory” and “Scientific research”. In other words, a real-world problem and solution have to be translated into academic research.

Design Science Research (DSR) is the proposed research methodology as it combines both design and research in one method, as set forth by Hevner [14]. DSR uses both design research (DR) and scientific methods to acquire new knowledge by incorporating previous ideas [15].

Understanding the problem is fundamental to the implementation of a design artefact. The solution therefore calls for validation of the research problem within a real-world domain and consequently the solution to this real-world problem by following a rigorous process, as all results have to undergo rigorous verification and validation.

DSR also allows for the presentation of new knowledge in an effective academic manner, to both technology-oriented and management oriented audiences [14].

The methodology addresses the following aspects:

1. Primarily a problem is going to be addressed - as a result a physical design artefact will be developed / created using DSR;
2. Secondly, new knowledge will be acquired and added to the current knowledge base;
3. All research will be done in a systematic, scientific manner, using both scientific and experimental methods;
4. Finally, DSR requires the research knowledge to be presented in a well-formulated academic format, as presented in this research document.

2.1 Design science research

From this point forward DSR will be discussed as the main design and research framework. In 2004 Alan R. Hevner [14] introduced DSR as a problem-solving paradigm in the domain of information technology (IT). DSR comprises a set of analytical tools and techniques with the goal of problem-solving in a structured, effective manner. The framework focuses on the development of physical and abstract artefacts and meta-artefacts, solving real-world problems in an analytical manner, and employs a creation and evaluation method. The method relies on rigorous scientific and engineering design principles.

DSR works by systematically converting a real-world problem into a research problem and theoretical framework. This framework is then used to analyse the research problem in an academic domain, making use of existing academic literature and other references in the process.
As a result, a deepened understanding of the problem is achieved and the knowledge needed to formulate a solution is expanded upon.

### 2.2 DSR environment

The goal of DSR is the creation of a solution artefact, that is, an innovative solution intended to accomplish a goal within an operational environment. The solution needs to satisfy predefined requirements whilst being subjected to operational constraints. To further explain the DSR process, the research environment is shown as an IDEF0 process block:

![Figure 2-1 DSR IDEF0 context](image)

#### 2.2.1 Research inputs

The input to the DSR process is the need: “A need exists for an autonomous neutron monitor for use in a low-temperature environment”. The inputs are thus the client’s primary need for counting neutrons and all environmental requirements associated with that need.

#### 2.2.2 Research outputs

DSR can deliver both physical and academic artefacts. Therefore, all outputs of the research process will be grouped into four distinct types:

**Constructs - artefacts**

The primary output for the research will be a constructed is a Neutron Monitor data acquisition sub-system. Mainly the data registration system that consists of a physical electronic system – as the primary artefact of this research.
Instantiations - artefacts

Instantiations are operationalized constructs, models and methods in the problem environment. The electronic sub-system was identified as the most risky part of the development due to its complexity and unknown challenges at the onset of the research process. Due to limited budget and a predefined scope of work, a final integrated product was not delivered. Therefore, the final instantiation will form part of an industrialization effort in a future project.

Models – meta-artefacts

A model is an abstract construct of a physical entity. This can be a theoretical description of an observable relationship between a construct and its environment, for example. In this research the model output will be divided into two types:

1. System development modelling: a set of models consisting of theoretical designs. Vital to the research is the design process and reproducibility in a manufacturing phase. For this reason, computer aided designs (CAD) had to be generated for future development and manufacturing processes. These models include mechanical and electrical CAD models;

2. System operational characteristics, where the behaviour of the artefact within its environment had to be modelled. This includes temperature effects and power consumption characteristics. These models represent the expected behaviour of the system in operation.

Methods – meta-artefacts

A method, as an output of the research process, describes all steps and associated guidelines used in the process of creating the abovementioned models and artefacts. The design process will be described in detail in Section 6 as this is a method of interest.

2.2.3 Research resources

Observations from prior efforts

The system to be researched and developed is based on the existing MNM, derived from the calibration neutron monitor (CNM) developed by the CSR in 2003 [2]. The existing MNM will consequently be evaluated as a possible solution to the need for low temperature, autonomous operation. The existing infrastructure will also serve as a verification tool - comparing any new system’s performance against the existing system’s performance.

The MNM was first proposed in work done by H. Kruger [2] and R. Fuchs [1]. The MNM Data Acquisition System (MNM-DAS) design methods [1] used by Fuchs served as a starting point for the MNM design evaluation.
Experience

Interviews with the expert field practitioners helped to identify relevant problems and issues [16]. The NWU CSR department served as an expert knowledge base.

Literature study

Excluding the existing system, new knowledge with respect to processes, techniques, models, and methods relevant to the research topics were needed in the following fields:

- Low power design (electronic);
- Low temperature design (electronic and mechanical);
- Power systems (electronic).

These literature topics are also relevant to the validation of the proposed solution.

2.2.4 Research controls and constraints

Environmental

One of the design requirements is a lower operating temperature of -60 °C. The reason is that the system will be deployed in an unsheltered, high-altitude, low-temperature location, i.e. the system had to be developed for low temperatures.

Cost

As mentioned by Kruger [2], the MNM was developed as a smaller, less costly NM. The new system - from this research - will inherit the same design specifications. System cost will therefore be a design constraint.

Technology

Based on the constraints above, technology to be used will be determined by temperature and cost constraints.

Verification and evaluation constraints

Normally, verification includes analysis, testing, demonstration and finally, deployment. Within the design evaluation phase it is necessary for “testing to confirm” and “testing to learn” whether a technology will be able to satisfy a particular requirement.

An excessively detailed simulation of a low-temperature environment becomes impractical at some point as a simplified model provides results beyond a point of diminishing returns. Available cold-chambers at the NWU lacked the capacity in terms of physical volume and testing was limited to theoretical modelling – this is not a major shortfall since thermodynamics is a known field and assumptions can be made without introducing major error.
Operational lifetime testing was also found to be impractical due to available development time and logistical constraints. Therefore long term final product testing will be validated within the deployment phase, which was defined to be beyond the scope of this research.

2.3 Three-cycle view

With all the inputs and outputs shown in the previous section, the following discussion is focussed on the flow in the DSR process flow. Shown in Figure 2-2, Hevner [14] created the “Three-Cycle Framework” to structure and define design problems into three domains: environment, design science and the knowledge base. These domains are linked by three processes, namely the relevance cycle, the design cycle and the rigor cycle.

![Three-cycle view of DSR](image)

*Figure 2-2 Three-cycle view of DSR [17]*

It is worth noting that the three cycle view has no specific entry point and consequently should be viewed as an interaction between three separate processes across three domains. Whilst each process has dependencies, they are independent during execution.

2.3.1 Design cycle

The design cycle forms the core of DSR and will be discussed first. The objective of this cycle is to construct a design artefact and refine it before it can be deployed. This artefact is created by first creating solution alternatives which are then evaluated against each other. Thereafter, the design is refined and updated requirements are generated.

Within the design cycle is an evaluation process that requires rigorous and engineering-scientific testing of artefacts before field testing. Failure to validate a design can lead to
unnecessary time being spent going back and forth between design and implementation. The result may have financial consequences that lead to a project’s ultimate failure.

During the research, a low-power MNM capturing system was produced, but rather than generating a complete system with alternatives to the system, the system was reduced to sub-systems (systematic breakdown) and lower-level alternatives were considered.

The requirements and constraints of each subsystem were used for evaluation of the artefacts [20], thus the need for a rigor cycle and the relevance cycle was identified. Figure 2-3 shows the design cycle with inputs and outputs connected to the other cycles.

The design cycle is independent from the other cycles, but it interfaces to the relevance and rigor cycles in order to ensure validation and verification [18]. This cycle uses theories and methods established by the rigor cycle. Furthermore, requirements and constraints are established within the relevance cycle. It is only after the artefact has been operationalized that new requirements and constraints can be updated, validating the artefact within the environment.

It is from both the design and evaluation loop and the implementation phase that new knowledge is acquired, essentially yielding an artefact and associated knowledge.

**Artefact creation**

Steps to create an artefact are discussed below:

*Determine design methods required*

A new MNM design had to be identified at the onset of this research. As a starting point, the initial design required three considerations: power consumption, temperature reliability and automated operation. Requirements were defined and researched as part of a literature study.
Identify suitable technology

This step required identification of suitable (fit-for-purpose) technology that addressed all design requirements identified earlier. Thereafter, alternatives were researched as part of a literature study.

Create alternatives

The system had to be reduced to functional units. Each alternative could be viewed as a sub-problem requiring its own DSR design cycle with solution alternatives. Throughout the design process, each sub-system decision had to be validated.

Evaluate system based on the three primary requirements

Each sub-system was assessed with experimental testing, yielding performance and validation data.

1. Functional capabilities: The characteristic of the system was evaluated through experimental testing, therefore each unit’s performance was verified;

2. Power consumption: The research requirement was first to establish the monitor power rating. An experiment had to be conducted to determine the current system power consumption. Each peripheral had to be tested separately and with different operating conditions to determine the total system energy requirement. The system sample rate versus power consumption had to be measured;

3. Temperature: Research into low-temperatures components had to be done. Failure and performance characteristics established. Because of limited testing equipment, specifically refrigeration units large enough to test the system, evaluation was limited to design choices and manufactures’ specifications, as was discussed in literature. In the case of some of the smaller modules, a low-temperature operating test was performed to establish the modules operational limits.

Optimization / Refinement

From the tests and evaluations above, system characteristics could be derived. Certain system components could be redesigned or acquired, whilst other legacy components had to be used as constraints imposed from a limited budget.

2.3.2 Relevance cycle

“Design science research is motivated by the desire to improve the environment by the introduction of new and innovative artefacts and the processes for building these artefacts.” [14]
The relevance cycle is responsible for three main functions in the DSR process:

Firstly, the relevance cycle provides the requirements for the research. By decomposing a problem into simplified sub-problems, it becomes possible to define research topics relevant to the larger research challenge.

Secondly, acceptance criteria needed to evaluate research are defined. The implementation of physical design validates the artefact along with the simulation, consequently stimulating improvements. Results obtained from field testing show sub-system and system characteristics, possibly also showing deficiencies in requirements. Any claimed improvement must be measured and validated by a relevance cycle.

Thirdly, the design still needs to be relevant. This is assessed by asking the following questions, namely: “Does the problem still exist?” “Is the solution still relevant?”, and “Is the solution cost-effective within an acceptable level of risk?” If a solution has no relevance, there would be no need for that solution in the real world.

2.3.3 Rigor cycle

The rigor cycle refers to rigorous implementation from the effective use of methods, knowledge, and techniques [14]. Through research and referencing of prior knowledge, a selection of appropriate theories and methods is used to implement a design. DSR is a scientific method subjected to appropriate data collection and analysis techniques.

Thus, the rigor cycle requires application of all necessary techniques, methods and knowledge used to develop a new artefact. At the same time, the rigor cycle feeds back into the knowledge base, showing that experience is gained through the acts of construction and meta-artefact creation. As a result, the knowledge base is enriched.

2.4 DSR guidelines

To verify the use of the DSR methodology Hevner [14] suggested seven guidelines as a structure to DSR.

1. Design as an artefact - DSR must produce a viable artefact in the form of a construct, a model, a method, or an instantiation;
2. Problem relevance - The objective of DSR is to develop technology-based solutions to important and relevant business problems; Pre-evaluation on the problem relevance has to be conducted;
3. Design evaluation - The utility, quality, and efficacy of a design artefact must be rigorously demonstrated via well-executed evaluation methods;
4. Contributions - Effective DSR must provide clear and verifiable contributions in the areas of the design artefact, design foundations, and/or design methodologies;
5. **Research rigor** - DSR relies upon the application of rigorous methods in both the construction and evaluation of the design artefact;

6. **Design as a search process** - The search for an effective artefact requires utilizing available means to reach desired ends while satisfying laws in the problem environment;

7. **Communication of research** - DSR must be presented effectively to both technology-oriented as well as management-oriented audiences.

### 2.5 Research knowledge contribution

A contribution inherently implies the creation of something new, but fundamentally nothing is really “new” [18]. Everything is made up from something else, that is to say, constructed or derived from previous ideas in a constructivistic way. To identify a knowledge contribution, the nature of a design must first be assessed. The audience to whom it is communicated also plays a role in the assessment of the term “new”. The maturity of an idea is presented by Figure 2-4.

#### 2.5.1 Maturity of this research contribution

Maturity refers to the research in terms of both problem maturity and solution maturity. Figure 2-4 shows the solution versus the problem domain. The matrix provides an indication whether a solution is innovative or simply a repetition in a routine manner.

As the low-power MNM is an improvement on the existing MNM, expected to operate in a new environment, there were known and unknown challenges at the onset of this research. In Figure 2-4, as shown in the highlighted area, the research contribution was classified as an improvement to a known problem.

![Figure 2-4 Maturity of this research contribution](attachment://image.png)
2.5.2 Contribution

The research contribution can be grouped into three distinct areas:

1. *Low power design* - the field of low power systems design will be enriched by the contribution in design techniques required to lower power consumption. Although this field is already extensively researched, the field of automated scientific observatories will benefit from new knowledge acquired in the field;

2. *Low temperature design* - in conjunction with the previous contribution, there is still limited research in the field of harsh-environment monitoring. Therefore the field still has scope for development in the development of neutron monitors, specifically;

3. *Autonomous design* - the scientific research community is constantly looking for new means of acquiring observation field data. With the limited resources of the current budget, the development of low cost automated observatories is fundamental to future research.

2.6 Conclusion

The research focuses on the design of a new neutron monitoring data acquisition system as a physical artefact, with specific focus on the electronic sub-system design as it posed significant initial risk. Therefore, the point of research entry had to be “objective focused”, as indicated by Figure 2-5. Consequently, this research delivers new design knowledge required in the development of an MNM-DAS system, including all relevant methods, old and new. As a design project, the actual device is of importance, but it has no value as a “single unit” if it cannot be reproduced or developed further. Therefore the outcomes of this research are also designed models and all methods, theories and techniques that were used as meta-artefacts.

This contribution, therefore, allows future work in autonomous neutron monitor development, not only for the improvement of this artefact, but also for the improvement of the knowledge base.
2.6.1 DSR process

To embed the design methodology process, the above discussion on DSR and its cycles is used to show how DSR was applied to the synthesis and evaluation of an MNM as set out below. The application of DSR to the neutron monitor research and development also shows the work that was done to address the initial need:

**Relevance cycle 1**

1. **Problem identification**
   - Identify low-power MNM relevance and justify the value of an improved design based on the original MNM, motivating the research to both a scientific and engineering audience.
2. **Define objectives**
   - Determine performance objectives for a solution (requirements);
   - Identify research topics (broadly) as well as design techniques and methods;
   - Identify resources required to conduct this research and development.

**Rigor cycle 1**

3. **Literature review**
   - Identify research topics and methods to address the design and development of a low-temperature, autonomous neutron monitor.
Design cycle

4. Design an artefact
   - Create a physical artefact – the electronic sub-system for the MNM;
   - Provide a conceptual design of the overall MNM, including mechanical design;
   - Formulate design alternatives to meet functional and performance objectives;
   - Evaluate design alternatives and select appropriate solutions.

5. Design evaluation
   Artefacts should be evaluated based on the specific requirements, by demonstration of the following evaluation processes:
   - Use laboratory experiments to characterize the system;
   - Compare the new system to the existing systems to show improvement.

Relevance cycle 2

6. Problem relevance
   - Evaluate whether the design artefact is relevant, that is, does the artefact meet the defined requirements?

7. Design as a search process
   - Search for a solution (possibly constructed from existing solutions in a constructivistic way) that adheres to budget and time constraints.

Rigor cycle 2

8. Research contributions
   - Show relevant improvement with respect to the existing MNM.

9. Communication of research
   - Communicate the problem and its importance to a wider audience, as is done in this thesis;
   - Show the utility of the developed artefact – the data acquisition sub-system – through its performance (test and evaluation).

2.7 Summary and document outline

Design science research was introduced as the research methodology applied in this research. A definition of DSR was provided, after which the application of DSR to the development of a low-power, low-temperature neutron monitor was presented. The development of an improved data acquisition sub-system for a new generation of neutron monitors was shown to benefit from the DSR process as this process creates artefacts and meta-artefacts that can be used in future developments.

An objective-focused entry is made into the DSR process with a clear contribution in the form of an improvement on an existing problem (improvement to a known problem).
For the sake of clarity, specific steps in the DSR process were listed above to show the work that was done in this research. The outline as shown in the figure below shows how chapters of this thesis align with the DSR process:

**Figure 2-6 Document outline in the DSR context**
3 Problem analysis

The purpose of this research was defined to be the synthesis and evaluation of a low-power MNM for use in a low-temperature environment. Additionally, the system is required to be autonomous in order to function as a remote observatory.

The existing MNM is dependent on external power and therefore inadequate as an autonomous observatory. Additionally, the existing system characteristics - to be discussed in the following section - show that not all system components were rated for a low-temperature environment. Therefore, the system had to be replaced with an upgraded version.

The existing CNM and MNM systems are reviewed in the following sections, followed by requirements for the new system.

3.1 Calibration monitor

In 2002 two CNMs were built for the purpose of obtaining global rigidity spectra. Their mobile design facilitated latitude surveys that helped to validate the cut-off rigidity for worldwide stationary NMs, subsequently allowing accurate calibration of these monitors [19].

The CNM consists of two primary functional blocks, namely a counter body and a data acquisition system (DAS). Figure 3-1 shows a photograph of the calibration monitor with the DAS attached to the body.
3.1.1 Counter body

The core of the NM is a proportional counter. The counter is responsible for the physical observation of neutron particles, producing small current pulses for each neutron particle event detected.

![Calibration body components](image)

**Figure 3-2 Calibration body components**

**Components**

As described by Kruger [2], the body is made up of the following sub-components:

*Reflector*
Polyethylene (CH$_2$) is used for the reflector material, with an outside diameter of 350 mm, a wall thickness of 78 mm, length 753 mm and a reflector weight of 42.5 kg.

*End plate*
The two ends of the reflector are covered with two polyethylene caps, each 50 mm thick.

*Producer*
The producer consists of seven lead rings, each ring having an outside diameter of 192 mm, a thickness of 45 mm, a length of 93 mm and total weight of 145 kg.

*Moderator*
The moderator consists of a pipe of polyethylene (CH$_2$) with a diameter of 99.5 mm, thickness of 19.5 mm and a length of 675 mm.

*Counter tube*
The proportional counter is a gas filled Geiger Muller (G-M) counter, of which the CNM uses a $^3$He counter tube instead of the $^{10}$BF$_3$ counter commonly used within a NM64 monitor. The
3He counter has sensitivity (counting rate per unit time) of 9% compared to an NM64 counter. Work done by Moraal [19], showed that given a high-latitude sea level location, a CNM would give a counting rate of ≈ 1 Hz and at lower latitudes at sea level a CNM would yield a counting rate of ± 0.5 Hz.

There are four counter tube variants that can be used. All are one third the length of the standard NM64 counter. Table 3-1 shows all these counters and for comparison purposes, also the specifications of the NM64 and IGY in the last columns.

<table>
<thead>
<tr>
<th>Table 3-1 MN Counters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Counter type</td>
</tr>
<tr>
<td>Fill gas</td>
</tr>
<tr>
<td>Fill gas</td>
</tr>
<tr>
<td>Fill pressure</td>
</tr>
<tr>
<td>Operating pressure</td>
</tr>
<tr>
<td>Operating temp</td>
</tr>
<tr>
<td>Length</td>
</tr>
<tr>
<td>Diameter</td>
</tr>
<tr>
<td>Absorption path length</td>
</tr>
<tr>
<td>Sensitivity</td>
</tr>
<tr>
<td>cps/nv</td>
</tr>
</tbody>
</table>

As shown by this table, each tube has a defined fill gas, gas pressure, diameter, optimum voltage and sensitivity. The sensitivity $nv$ is defined as the sensitivity to one thermal neutron per square centimetre per second.

**Cradle**

The combined weight of the MNN body is 201.3 kg; it is therefore logistically too heavy to be moved by hand. Thus, a trolley is used to move the body. The cradle weighs 21.5 kg and is used to secure and transport the MN body.

### 3.1.2 Data acquisition system

The second system block is that of the data acquisition system (DAS). The CNM has a cylindrical enclosure secured to the front of the monitor body. The enclosure contains the following system components [19]:

[19]: Reference number
Embedded PC:
All the computing of the DAS is done by means of a 486 (x86) architecture embedded PC.

Low-voltage power supply:
Most of the subsystems need 5 \(V_{DC}\) and 12 \(V_{DC}\), to function. An ATX industrial computer power supply is used to convert 220 \(V_{AC}\) to the required voltages.

High-voltage power supply:
The GM counter tube needs to be biased with a high voltage potential. Therefore a high-voltage DC/DC converter is needed.

Data storage:
The system uses a 20 GB removable IDE hard drive to run imbedded PC operating systems and store all the recorded data.

Pressure sensor:
The atmospheric air pressure is measured using a built-in Paroscientific solid-state barometer, with an accuracy of \(\sim 0.1\) mmHg.

Temperature sensor:
As the monitor is temperature dependent, the system uses a temperature sensor to make temperature corrections.
**GPS unit:**
The function of the CNM was a latitude survey of counting rates at different locations, thus there was a need to know the monitor’s location at any given time. For that reason a GPS unit was used.

**A/D module:**
The G-M tube produces small voltage pulses in response to neutron detection events. Therefore, a module is needed to amplify these pulses and convert them into a digital format used by the embedded PC to sample such a neutron event. An op-amp pre-amplifier is used to increase the pulse voltage and thereafter additional circuitry is used to shape and transform the analogue pulse to a digital pulse.

**External UPS:**
 Optionally, an uninterruptable power supply can be used to power the system in case of power outages.

### 3.1.3 Environmental effects

The CNM was designed to function inside a controlled, indoor environment. There is a significant factor that affects the system performance, namely the temperature effect on counter sensitivity.

**Temperature sensitivity**

It was found that differently designed NMs had different temperature responses [22]. A $^3$He NM was found to be four times more sensitive to temperature than a $^{10}$BF$_3$ monitor. The overall temperature coefficient of any NM was determined by the separate coefficients of the reflectors, lead producers, moderators and counters. The reason for different temperature coefficients is explained by the different cross-sections of the detector gases. The calibrator has the largest sensitivity, followed by the $^3$He 3NM64, the IGY and thereafter the $^{10}$BF$_3$ 3NM64. The following table shows documented monitor temperature sensitivities.

<table>
<thead>
<tr>
<th>Neutron Monitor</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^3$He Calibrator</td>
<td>$0.118 \pm 0.005 % / ^\circ C$</td>
</tr>
<tr>
<td>$^3$He 3NM64 (Thule/Nain)</td>
<td>$0.091 \pm 0.002 % / ^\circ C$</td>
</tr>
<tr>
<td>$^3$He 3NM64 (Simulation)</td>
<td>$0.073 \pm 0.007 % / ^\circ C$</td>
</tr>
<tr>
<td>$^{10}$BF$_3$ IGY (Potchefstroom)</td>
<td>$0.053 \pm 0.012 % / ^\circ C$</td>
</tr>
<tr>
<td>$^{10}$BF$_3$ 3NM64 (Thule)</td>
<td>$0.044 \pm 0.002 % / ^\circ C$</td>
</tr>
<tr>
<td>$^{10}$BF$_3$ 3NM64 (Simulation)</td>
<td>$0.018 \pm 0.006 % / ^\circ C$</td>
</tr>
</tbody>
</table>

It is therefore preferable to use a $^{10}$BF$_3$ NM, in environments with small temperature variance.

### 3.1.4 Summary

From this calibration design, the idea of an MNM emanated, used not only for calibration but also as a smaller replacement version of the full-size NM64 monitor.
3.2 Mini neutron monitor

This section describes the design and system layout of the work done by Fuchs [1], who proposed and redesigned the CNM electronics to produce an MNM. The MNM design was motivated by the difficulty and expense of deploying full-sized NMs. This was due to the higher sensitivity of the NMs. The original CNM used a $^3$He G-M tube, but, due to increasing prices of $^3$He, it was decided to revert to $^{10}$BF$_3$ G-M tubes. The $^{10}$BF$_3$ tube is less sensitive than the $^3$He tube, but has the benefit of producing higher energy pulses per event than a $^3$He tube.

In 2011, the electronics of the calibration monitors were completely redesigned, leading to the expanded concept of an MNM. The first of these was deployed on the German Polar research vessel, the Polarstern in December 2011. A second stationary MNM was installed on the German Antarctic station, Neumayer III, in February 2012.

The following illustration shows a modular view of the MNM DAS:

![Modular view of MNM data acquisition system](image)

**Figure 3-4 Modular view of MNM data acquisition system**

3.2.1 Functional abstract of the MNM DAS

The MNM DAS can be divided into six functional groups.
**Counter**

The fundamental function of a MNM is detection of thermal neutron particles. This is achieved by Functional Unit (FU) 1, a gas-filled proportional counter tube. The MNM interfaces with either a $^3\text{He}$ or a $^{10}\text{BF}_3$ proportional counter. This requires a stable high voltage source, provided by FU 2. The High Voltage Supply FU 2 establishes a strong electric field within the counter tube.

In the event that a thermal neutron is detected, the proportional counter produces a small current pulse. The pulse is then amplified to a usable voltage by the pre-amplifier, depicted by FU 3.

**External sensors**

Along with neutron detection, additional sensor data is needed. Temperature, atmospheric pressure, location and the precise time all contribute to the neutron monitor dataset. A time-keeping module, FU 5, provides accurate timing for the system.

---

**Figure 3-5 MNM DAS functional abstract**

The diagram illustrates the flow of data and components involved in the MNM system. The Neutron event triggers the Proportional counter, which generates a small current pulse amplified by the Pre-amplifier. This pulse is then processed by the Discriminator, and the result is displayed along with indicators. The User I/O module allows for input, and the Data storage unit involves an Ethernet controller and a USB flash drive.
The counting rate is dependent on the temperature and atmospheric pressure of its environment. Therefore, a temperature sensor FU 6 and a pressure sensor FU 7 are used. The system records temperature to within 1 °C [1].

**User I/O**

A display - FU 10 - gives user feedback as to the system status and modes. Along with this feedback, the user is capable of issuing commands to the system using buttons (FU 9).

**Data storage**

A capturing system generates data. The data is stored by one of the two modules, FU 11 or FU 12. Data is stored either through the Ethernet module FU 11 on a network location, or internally within a USB flash drive FU 12.

**Control unit**

All the pervious groups provide either input or output sensory data. To manage these interfaces, a central control unit FU 4 is used to capture all data. All data is processed and transferred to a storage group.

A second function of FU 4 is discrimination of amplified pulses. Each pulse amplitude conveys information on the neutron particle detected. This is used to validate the detected neutron in order to reject spurious noise pulses that may be misinterpreted as valid events.

**Power management unit**

The last group to be discussed is the power management system. Each previous group has unique power requirements. Therefore, FU 8 provides the individual voltages needed for each subsystem. By means of DC/DC converters, a single input voltage is converted to applicable sub-system voltages.

### 3.2.2 MNM system specifications

The MNM function-to-resource allocation as presented and demonstrated by Fuchs [1], are shown below:
A discussion of characteristics of the different sub-systems follows below.

**Low-temperature performance**

To test the MNM low-temperature performance, the complete capture system was exposed to an operating temperature of -40 °C. Only the LCD display showed visible temperature effects - freezing and locking up. Other than the LCD display, no detrimental effects were observed running the system at low temperatures. As some of the sub-system modules are rated only down to 0 °C, the only conclusion that can be made from the above test is that for specific modules the mean time to failure (MTTF) at low temperature would be reduced.
Shown in Table 3-4 are the individual modules and their respective operating temperatures.

Table 3-4 MNM temperature ratings

<table>
<thead>
<tr>
<th>G-M tubes</th>
<th>Minimum operating temperature (°C)</th>
<th>Effect @ -40 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>LND20366 10BF3</td>
<td>-55</td>
<td>Britteness, reduced shock handling</td>
</tr>
<tr>
<td>Spellman HV</td>
<td>0</td>
<td>MTTF reduced</td>
</tr>
<tr>
<td>Amplifier</td>
<td>-40</td>
<td>Non-linearity results</td>
</tr>
<tr>
<td>PIC32MX</td>
<td>-40</td>
<td>No observed or published effects</td>
</tr>
<tr>
<td>Basic devices</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Crystal Oscillator</td>
<td>-40</td>
<td>Stops functioning</td>
</tr>
<tr>
<td>Pressure Sensor</td>
<td>-54</td>
<td>Non-linearity results</td>
</tr>
<tr>
<td>Temperature Sensor</td>
<td>-10</td>
<td>Non-linearity results</td>
</tr>
<tr>
<td>LCD</td>
<td>-20</td>
<td>Display stops working</td>
</tr>
<tr>
<td>DC/DC Converter</td>
<td>-40</td>
<td>Efficiency stops working &amp; Oscillator fault</td>
</tr>
<tr>
<td>PCB (FR4)</td>
<td>-55</td>
<td>Britteness, reduced shock handling</td>
</tr>
<tr>
<td>Polycarbonates Box</td>
<td>-40</td>
<td>Britteness, reduced shock handling</td>
</tr>
</tbody>
</table>

Sub-system power consumption

Table 3-5 shows the power requirements for each MNM sub-system, as rated by [1].

Table 3-5 MNM power usage

<table>
<thead>
<tr>
<th>Basic functions</th>
<th>Measured power</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Current (mA)</td>
</tr>
<tr>
<td>FU 1: Counter tube</td>
<td>0</td>
</tr>
<tr>
<td>FU 2: High-voltage</td>
<td>40</td>
</tr>
<tr>
<td>FU 3: Pre-amplifier</td>
<td>1</td>
</tr>
<tr>
<td>FU 4: Micro-controller</td>
<td>200</td>
</tr>
<tr>
<td>FU 5: GPS</td>
<td>70</td>
</tr>
<tr>
<td>FU 6: Pressure sensor</td>
<td>1</td>
</tr>
<tr>
<td>FU 7: Temperature sensor</td>
<td>1</td>
</tr>
<tr>
<td>FU 9: User IO input</td>
<td>25</td>
</tr>
<tr>
<td>FU 10: LCD &amp; LEDs</td>
<td>30</td>
</tr>
<tr>
<td>FU 11: Primary storage</td>
<td>100</td>
</tr>
<tr>
<td>Ethernet</td>
<td></td>
</tr>
<tr>
<td>FU 12: Secondary storage</td>
<td>18</td>
</tr>
<tr>
<td>USB</td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
</tr>
<tr>
<td>FU 8: Power management</td>
<td>101</td>
</tr>
<tr>
<td>(80% Efficiency @ 2.01W)</td>
<td></td>
</tr>
<tr>
<td>Average power consumption</td>
<td>502</td>
</tr>
</tbody>
</table>

The power consumption is significant when considering autonomous operation. This must be addressed as part of a low-power design.
Logistic requirements

The MNM was developed to be deployed in an indoor environment with external mains power available. Therefore, the system was not designed to be exposed to outdoor environmental hazards, such as low/high temperatures, high humidity and dust particulates.

An additional constraint is that the system’s primary data storage is an Ethernet-connected FTP server.

System capability and shortfalls

Although the system can operate automatically to a certain degree, the following aspects limit its autonomous application in a remote, low-temperature environment:

- The system runs off an external power source, namely an external 5 V DC supply connected to 220 V AC;
- The data storage is primarily Ethernet-based;
- Some of the sub-system components are not rated for operating in -40 °C;
- The system is not protected against external particulates such as water and dust;
- The system excessively uses power, making a battery operated conversion impractical.

The MNM system is thus incapable of operating autonomously. As a result, the new system had to be improved to meet the new requirements. There were, however, existing architectural design options that were fixed because of historical component design and purchasing choices, including:

- The LND G-M proportional counter: this is the most expensive component of the design and alternatives would have been costly considering the project already had existing stock;
- A pressure sensor. The existing MNM used one of two devices, a Paroscientific Pressure Sensor or a Vaisala Pressure Sensor. These were also existing stock items. Taking cost into account, they were fixed within the new design.

3.3 General neutron monitor configuration

Using the two systems described above, an NM can be generalized as a set of basic functional units:

- Power supply:
  - Low voltage;
  - High voltage;
- Signal Processing:
  - Pulse amplification;
  - Sampling (analogue/digital conversion);
- Time and location awareness;
- Pressure sensing;
- Temperature sensing;
- Computation and control;
- Data storage.

Accordingly, Figure 3-6 shows the interconnected functions in a functional architecture.

![Proportional mode](image)

**Figure 3-6 Basic neutron monitor architecture**

### 3.4 Problem statement

To summarize the problem statement:

*An MNM is needed that can operate in a low temperature, remote environment.*

#### 3.4.1 Problem

Higher altitudes lead to logistical support problems and lack of infrastructure. This limitation introduces the need for autonomous operation (the unit will be exposed outdoors) in a harsh environment. The problem statement can be defined as:
Research and develop an autonomous, low-power neutron monitor for use in a remote low-temperature environment

An important aspect is to make every effort to ensure requirements are unambiguous and verifiable as these will determine the artefact’s success.

3.4.2 Functional requirements

The above requirements imply the following minimum specifications. The monitor must:

- Measure cosmic ray neutron activity;
- Measure temperature;
- Measure atmospheric pressure;
- Provide an accurate internal date and time keeping system;
- Operate independently, off the electric mains/grid;
- Provide internal data storage.

3.4.3 Environmental requirements

- Must operate within temperature range of -65 °C to +30 °C;
- Must have ingress protection - be protected against dust and snow particles.

3.4.4 Performance characteristics

- Must operate independently for at least 12 months;
- Must be able to store one-minute-average samples on an internal memory system.

3.4.5 Logistical requirements

- The end-product / assembly should be kept within a reasonable size. The primary size constraint of the system is based on the fixed size of the MNM body. The existing body with a trolley serve as the minimum size of the system;
- The system should be easy to transport, therefore modular in design;
- The system cost should be kept to a minimum.

3.4.6 Usability requirements

- No user interaction or maintenance must be required;
- Data storage technology must be easily removable.

3.5 Research scope

The academic research will focus on the following topics:

*Extreme environmental conditions / challenges:*
Research into low-temperature electronics and the effects of prolonged low-temperature operation had to be done. Low-temperature materials, insulation and heating had to be researched.
**Logistic constraints:**
Due to logistical requirements, the scalability of the system had to be investigated. How to assemble and transport the system also had to be addressed.

**Limited budget:**
Research centres worldwide suffer from economic constraints, as was the case in this research. Therefore, cost played a role in component selection and design.

### 3.6 Conclusion

From the above problem analysis, it became clear that the existing and historical neutron monitors could not address the real-world problem as they were not designed with the environment, logistics, and autonomy challenges in mind. A new monitor had to be researched and developed to address the primary research challenge, namely:

*Research and develop an autonomous, low-power neutron monitor for use in a remote low-temperature environment*

After the problem was analysed, a number of individual challenges arose, as summed up in Table 3-6 below. The matrix shows how each source of information, as shown in the rows of the table, validated the research challenges, as shown in the columns.

### Table 3-6 Research problem validation

<table>
<thead>
<tr>
<th>Research challenges</th>
<th>Extreme environmental conditions / challenges</th>
<th>Operation in remote locations</th>
<th>Logistical constraints</th>
<th>Limited budget</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cosmic-ray physics</td>
<td>↑</td>
<td>↑</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Neutron monitor principles</td>
<td></td>
<td>↑</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Future development challenges</td>
<td></td>
<td>↑</td>
<td></td>
<td>↑</td>
</tr>
<tr>
<td>Previous system CMN/MNM</td>
<td></td>
<td></td>
<td>↑</td>
<td></td>
</tr>
<tr>
<td>Environmental observations</td>
<td></td>
<td>↑</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Economic research environment</td>
<td></td>
<td></td>
<td></td>
<td>↑</td>
</tr>
</tbody>
</table>

The matrix above will be used later in this document to link research challenges to the literature study, after which solutions will be proposed for each challenge.
4 Literature study

4.1 Introduction

This literature study addresses operational, environment and logistical system requirements. As from the DSR methodology, rigorous implementation of existing methods, knowledge and techniques is needed. Therefore this literature review will conduct research, and in doing so, will also select appropriate solutions, methods, techniques and technologies identified to compile requirements for a new artefact.

4.2 Thermal dynamics - thermal energy

4.2.1 Thermal considerations

One of the first problems identified in this research was the harsh operational environment. An environment is considered harsh when it causes damage to the system exposed to it over an extended period of time.

Some of the types of harsh environmental conditions include; water, humidity, extreme temperatures, ingress, vibration and physical impact. Additional electronic conditions include electrostatic discharge (ESD) and electromagnetic interference (EMI).

For this research, it is the extreme range of temperatures that is of importance. In general, a temperature range is considered extreme when a system is exposed to temperatures ranging beyond the parameters of -40 °C to 125 °C. Electronic components are categorised in five temperature categories:

<table>
<thead>
<tr>
<th>Type</th>
<th>Temperature range  °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>0 to 85</td>
</tr>
<tr>
<td>Industrial</td>
<td>-40 to 85</td>
</tr>
<tr>
<td>Automotive</td>
<td>-40 to 105</td>
</tr>
<tr>
<td>Extended</td>
<td>-40 to 125</td>
</tr>
<tr>
<td>Military</td>
<td>-55 to 125</td>
</tr>
</tbody>
</table>

To understand the effects temperature has on electronic systems, one must first understand the relevant topics of heat, conduction, convection and radiation.

Since temperature played such a significant role in this research, it was necessary to conduct a literature study on this topic. This information was used as a guideline for the new low-temperature design, and will also serve as a meta-artefact to support future development.

For the sake of completeness, a comprehensive study was conducted, as documented below.
Heat capacity

Temperature is viewed as an environmental state or condition which reflects the kinetic energy of molecules within a material. Heat, on the other hand, is not energy in itself but rather the flow of energy between two objects due to the difference in temperature.

Specific heat capacity, $C_s$, is defined as the amount of heat, $Q$, needed to raise the temperature of a substance by one unit, defined by the following:

$$C_s = \frac{Q}{m\Delta T}.$$  \hspace{1cm} (4.1)

This reflects the energy required to heat an object to a desired temperature.

Heat transfer

To heat or cool a solid object, energy must be transferred between either two solid objects or between the object and its environment, also known as *heat flow*. The fundamental unit of heat is joule ($J$), and can also be expressed in calories (cal), the amount of energy required to raise one gram of water from 14.5 °C to 15.5 °C. The relation between these units is:

$$1 \text{ cal} = 4.1860 \text{ J}$$

Heat transfer is achieved primarily through the following three main mechanisms:

Conduction

Thermal conduction is the transfer of energy due to direct contact between two bodies of material, and can also be viewed as thermal diffusion; this can also include a length of material and the transfer of energy within.
According to Joule’s conduction law [24], the amount of heat flowing is proportional to the temperature gradient, as expressed by:

\[ Q \propto T_H - T_L = \Delta T. \]

This amount is directly proportional to the surface area \( A \), and inversely proportional to the length \( L \) of the conducting medium:

\[ Q \propto \frac{A}{L} (T_H - T_L). \tag{4.2} \]

The remaining constant of proportionality is called the thermal conductivity, \( k \), such that:

\[ Q = kA \frac{T_H - T_L}{L}. \tag{4.3} \]

When a substance consists of multiple materials, such as shown in Figure 4-2, the effective conductivity is defined as:

\[ k_{cond} = \sum \left( \frac{k_n}{L_n} \right) A \left( T_H - T_L \right). \tag{4.4} \]

**Figure 4-2 Multiple conductive interfaces**

Here \( k_1 \) through to \( k_N \) represent the individual thermal conductivities along lengths \( L_1 \) to \( L_N \). From this it is possible to model the multiple conductive as a single conductive medium. Table 4-2 shows examples of materials with high conductivities:
Table 4-2 Conductivity of common thermal materials [25]

<table>
<thead>
<tr>
<th>Good conductors</th>
<th>Thermal conductivity W/ m · K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Class epoxy laminate</td>
<td>0.25</td>
</tr>
<tr>
<td>FR4 PCB</td>
<td></td>
</tr>
<tr>
<td>Concrete, dense</td>
<td>1.0</td>
</tr>
<tr>
<td>Silica</td>
<td>1.3</td>
</tr>
<tr>
<td>Lead</td>
<td>20</td>
</tr>
<tr>
<td>Steel</td>
<td>46</td>
</tr>
<tr>
<td>Carbon Steel</td>
<td>56</td>
</tr>
<tr>
<td>Brass</td>
<td>109</td>
</tr>
<tr>
<td>Aluminum</td>
<td>250</td>
</tr>
<tr>
<td>Gold</td>
<td>310</td>
</tr>
<tr>
<td>Silver</td>
<td>429</td>
</tr>
<tr>
<td>Diamond</td>
<td>2300</td>
</tr>
</tbody>
</table>

The purpose of this study is to optimize a system for operation at very low temperatures. Thus the system electronics must be kept warm, necessitating the need for insulation materials. Table 4-3 shows examples of good insulation materials that may be used to inhibit the loss of energy.

Table 4-3 Thermal conductivity of common insulation materials [25]

<table>
<thead>
<tr>
<th>Good insulators</th>
<th>Thermal conductivity W/ m · K</th>
<th>Operating temp (°C)</th>
<th>Thickness range (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rock Mineral Wool</td>
<td>0.033</td>
<td>-200 to 900</td>
<td>20 to 120</td>
</tr>
<tr>
<td>Nitrile rubber</td>
<td>0.04</td>
<td>-40 to 105</td>
<td>38</td>
</tr>
<tr>
<td>Rigid Polyurethane Foam</td>
<td>0.022</td>
<td>-180 to 110</td>
<td>15 to 150</td>
</tr>
<tr>
<td>Polystyrene Foam Extruded</td>
<td>0.025</td>
<td>-60 to 75</td>
<td>12 to 200</td>
</tr>
<tr>
<td>Polystyrene Expanded</td>
<td>0.033</td>
<td>-150 to 80</td>
<td>5 to 610</td>
</tr>
<tr>
<td>Polyethylene Foam</td>
<td>0.033</td>
<td>-50 to 105</td>
<td>6 to 32</td>
</tr>
<tr>
<td>Glass Mineral Wool</td>
<td>0.028</td>
<td>-200 to 450</td>
<td>15 to 150</td>
</tr>
<tr>
<td>Glass Wool (Aerolite)</td>
<td>0.04</td>
<td>-200 to 450</td>
<td>15 to 150</td>
</tr>
<tr>
<td>Fiberglass (Rigid)</td>
<td>0.033</td>
<td>-200 to 450</td>
<td>15 to 150</td>
</tr>
<tr>
<td>Vacuum Insulated Panel (VIP)</td>
<td>0.001 – 0.008</td>
<td>-170 to 120</td>
<td>10 to 50</td>
</tr>
<tr>
<td>AIR, elevation 10000 m</td>
<td>0.02</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Air</td>
<td>0.0116</td>
<td>-150</td>
<td>∞</td>
</tr>
<tr>
<td>Air</td>
<td>0.0160</td>
<td>-100</td>
<td>∞</td>
</tr>
<tr>
<td>Air</td>
<td>0.0204</td>
<td>-50</td>
<td>∞</td>
</tr>
</tbody>
</table>

Currently, the most common inexpensive insulation material used within refrigeration applications is either: Extruded Polystyrene or Rigid Polyurethane Foam, both of which exhibit thermal conductivities close to that of air. In extreme applications, such as cryogenic freezers, Vacuum Insulated Panels are used. The primary design consideration in choosing one of these technologies is thickness and cost.
Radiation

The second mechanism of thermal energy transfer is electromagnetic radiation. No medium is required to facilitate the transfer of radiated energy, making it possible within a vacuum. An object radiates energy into its immediate environment that absorbs or reflected energy. This process is shown in Figure 4-3, it is also worth noting that both the environment and individual objects have the ability to absorb, radiate and reflect radiation.

According to Stefan’s law [26], the amount of heat radiated, $P_{Rad}$, by an object is proportional to $T^4$:

$$P_{Rad} \propto T^4.$$ 

Therefore, the amount of heat radiated by a given surface with area $A$ is:

$$P_{Rad} = \sigma A T^4. \quad (4.5)$$

Where $\sigma = 5.6703 \times 10^{-8} \text{ W/m}^2 \cdot \text{K}^4$, called the Stefan-Boltzmann Constant. This law pertains only to so-called ideal black-bodies, which are perfect emitters and absorbers of heat. In practice, all substances have non-ideal properties, therefore an emissivity, $\varepsilon$, such that $\varepsilon < 1$. Therefore, the final radiation law is:

$$P_{Rad} = \sigma \varepsilon A T^4. \quad (4.6)$$

![Figure 4-3 Radiated energy exchange between two objects](image)

This shows the process of energy loss; nonetheless for actual transfer to occur, the objects or the environment must be able to absorb energy. The absorbed radiated energy can be expressed as:

$$P_{abs} = \sigma \varepsilon A T^4_{ENV}. \quad (4.7)$$
where $P_{\text{abs}}$ expresses the energy absorbed by the environment, 
$\varepsilon$ = emissivity of the surrounding environment, 
$A$= surface area, and 
$T$= environment temperature. 
Combining these expressions yields the rate of radiated energy transferred by:

$$P_{\text{net}} = P_{\text{abs}} - P_{\text{rad}}.$$ (4.8)

Therefore, the emissivity of both the radiating object and the absorbing environment or object must be known. A black-body is a perfect radiator and poor reflector. Conversely a “light” substance has high reflectivity and poor emissivity. Illustrated in Table 4-4 are some common electronic manufacturing materials and their respective emissivities.

<table>
<thead>
<tr>
<th>Material</th>
<th>Emissivity $\varepsilon$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Polished Silver</td>
<td>0.02</td>
</tr>
<tr>
<td>Polished Aluminium</td>
<td>0.04</td>
</tr>
<tr>
<td>Bright Tin</td>
<td>0.04</td>
</tr>
<tr>
<td>Rough Aluminium</td>
<td>0.06</td>
</tr>
<tr>
<td>Dull Nickel Plate</td>
<td>0.11</td>
</tr>
<tr>
<td>Stainless Steel</td>
<td>0.28</td>
</tr>
<tr>
<td>Steel</td>
<td>0.55</td>
</tr>
<tr>
<td>Oxidized Steel or Copper</td>
<td>0.78</td>
</tr>
<tr>
<td>Anodized Aluminium</td>
<td>0.80</td>
</tr>
<tr>
<td>Glossy Paint</td>
<td>0.89</td>
</tr>
<tr>
<td>Flat Paint</td>
<td>0.94</td>
</tr>
</tbody>
</table>

It can be seen that Polished Silver is a very good reflector, contrary to Flat Paint which is closest to a black-body, making it a good radiator and poor reflector. Therefore surrounding an object with a silver coated material would reduce the flow of radiated heat to a minimum.

**Convection**

The last transfer mechanism is that of convection, the process of heat exchange through fluidic movement. When a medium comes into contact with a thermal energy source, the medium transports the thermal energy by conveying the heated medium to a new location.

It is through conduction that a heat source transfers thermal energy to a medium. The heated medium changes particle temperatures, therefore particle density, leading to the flow of particles: this is convection. A second interface then absorbs energy, once again through the method of conduction.
Figure 4-4 Basic convection

Figure 4-4 illustrates the movement of a fluid between two solid interfaces as a result of a temperature gradient.

Convection can also be in two major forms, natural and forced, as shown in Figure 4-5. Cooling applications make use of forced convection, because their higher rate of thermal transfer. Forcing a flow of air across a heated material makes it cool faster than natural convection would allow, transporting thermal energy away from the material. Therefore, convection is directly proportional to the fluid velocity. In the case of natural convection this is buoyant vertical movement and with forced convection, the movement is due to forced flow. Convective heat flows can therefore be categorized in two ranges [28]:

- **Natural convection:** $1 \sim 25 \text{ W/m}^2 \cdot \text{K}$
- **Forced convection:** $20 \sim 300 \text{ W/m}^2 \cdot \text{K}$

Figure 4-5 Convection types

Fourier’s heat equation for convection states that the heat transfer, $q_C$, due to convection is related to the thermal transfer coefficient $\bar{h}$, the area $A$, and the temperature gradient $\Delta T$:

$$q_C = \bar{h} \times A \times \Delta T.$$  \hspace{1cm} (4.9)
However, unlike conduction and radiation, the thermal transfer coefficient cannot be expressed in a simple mathematical form.

Therefore, it is assumed that the low-power electronics will be cooled by means of natural convection. According to [29, 28], convective heat of printed circuit boards (PCBs) can be approximated to an industry accepted value of 10 W/m²K. However, because the design power output will be relatively small, the temperature gradient between the board and ambient environment is expected to be very low. Consequently, the calculation of the thermal transfer coefficient will be discussed and evaluated for smaller temperature differences.

A PCB inside an enclosure can be approximated to a horizontal heated surface, as shown by Figure 4-6.

![Figure 4-6 Thermal convection model](image)

From Newton’s law of cooling, the thermal transfer coefficient, \( \bar{h} \), is shown to be:

\[
\bar{h} = \frac{N_u \times k}{L_c},
\]  

(4.10)

where \( L_c \) = characteristic length, 
\( k \) = Thermal conductivity of the fluid, and 
\( N_u \) = Nusselt number, the ratio of “convective heat” to “conductive heat”.

Before the Nusselt number can be defined, the type of flow needs to be determined. Convective flow is divided into two categories, laminar flow and turbulent flow.

![Figure 4-7 Convection flow types](image)

According to [28], flow remains laminar when a body has a temperature gradient of less than
100 °C per 0.5 m, hence for low-power electronic equipment, laminar flow can almost always be assumed.

Thus using laminar flow, the Nusselt number can be shown to be:

\[ N_u = 0.54 \times (G_r \times Pr)^{1/4} + 0.15 \times (G_r \times Pr)^{1/3}, \]

(4.11)

\[ Pr = \text{Prandtl number}, \quad G_r = \text{Grashof number}. \]

The Prandtl number describes the ratio of viscosity to the thermal diffusion, and depending on the temperature, the Prandtl number for air ranges between 0.7 and 0.8. The second value needed is that of the Grashof number \( G_r \), described by:

\[ G_r = \frac{g \times L^3 \times (T_B - T_A)}{T_A \times \mu_k v}, \]

(4.12)

where \( g = \) gravitational acceleration constant, 
\( L = \) plate length, 
\( T_A = \)ambient temperature, 
\( T_B = \)plate temperature, and 
\( \mu_k v = \)kinematic viscosity.

Assuming ideal gas properties with kinematic viscosity of \( 15.68 \times 10^{-6} \) m\(^2\)/s, an air thermal conductivity of \( 0.024 \) W/m K, a length of 0.2 m and an incremental temperature range of 1 to 30 °C, the following set of coefficients was derived.

![Figure 4-8 Horizontal plate thermal transfer coefficients](image)

**Figure 4-8 Horizontal plate thermal transfer coefficients**

From this figure, it is clear that proportional to specific board-to-air temperature ratio, the thermal transfer coefficients may vary in the range of 4 W/m\(^2\)K to 14 W/m\(^2\)K.

Assuming a low-power system generates marginal thermal energy, the board to air temperature ratio will be presumed to be less than 1 °C. Hence, the thermal transfer coefficient, for a low-power system, can be estimated be approximately 4 W/m\(^2\)K.
4.2.2 Thermal insulation

Up to this point the concept of heat was discussed using the heat transfer models; a system’s heat loss can be described by the sum of all three mechanisms:

\[ Q_{Total} = Q_{Radiation} + Q_{Conduction} + Q_{Convection}. \]

To prevent the flow of heat, all three modes of transfer need to be addressed, inhibiting the transfer of energy to the exterior environment.

**Thermal Conduction**

To prevent the flow of energy via conduction, insulation is needed; therefore insulation of a specific thickness must be selected.

**Radiation**

A radiant barrier must be used to reflect radiation back to the interior of the enclosure, therefore wrapping the enclosure in a reflective envelope.

**Convection**

Finally, the effect of convection can be significantly reduced by preventing the flow of air within a system. Keeping the air and enclosure volume relatively small will limit the flow of air. This effectively creates a homogenous temperature distribution within the air volume.

4.3 Electronic behaviour at low temperatures

The system requirement specifies a system for use in a low-temperature environment of well below -55 °C. The device will potentially be deployed in high-altitude Antarctic locations; for that reason the device has to survive extreme cold, high wind speed, total darkness and relative low humidity. The average electronic system is rarely expected to operate in conditions below -40 °C. Common electronics are grouped into predefined temperature ranges, as was shown in Table 5.1.

4.3.1 Ratings

Manufacturers commonly rate electronics to function within in certain specifications. These specifications are meant to quantify the quality and reliability of devices. Originally these ratings were meant to differentiate components by application.

One of the first specifications is that of the “recommended operating conditions” (ROC), the optimal operational conditions for a component:

- “Recommended operating voltage”;
- “Recommended operating temperature”;
- “Recommended start conditions”: a component has an inherent self-heating ability. Start-up currents combined with power dissipation create a transient response after being switched on, which differs for different starting temperatures [35]. Therefore, a
warm component will have a different start-up response to that of a cold component. A second set of specifications is that of “Absolute Maximum Ratings” (AMR). These ratings provide a guarantee that the component will function within minimum and maximum tolerated conditions, assuring acceptable reliability rather than efficiency [30].

- **“Operating voltage”**, is the minimum and maximum tolerated voltage the component can handle. The specification may also state the component performance as a function of the voltage. Additionally, any voltage beyond this range will lead to damage and consequent failure of the device.

- **“Voltage tolerance”**, where the device is used to interface with external devices or sensors, an interface tolerance voltage is specified; some functions may operate above or below the standard operating voltage.

- **“Maximum current ratings”**. Devices rarely function in isolation, but are usually connected to supporting components. These interfaces act as loads, drawing power from the device. If the interface exceeds the ability of the device to source electric current, the device may be damaged. Thus, the designer must be aware of current ratings whilst designing supporting circuits. A commonly neglected current specification is also the total current rating. In case of multiple IO pins, the sum of the currents sourced may not exceed the device’s internal maximum input current draw.

- **“Temperature tolerance”**. A device may be subject to varying temperatures either from the external environment or from internal heating. This rating guarantees that the device operates within specification; beyond this a component may be subject to failure, reduced MTTF and unpredictable behaviour. Referring back to Table 4-1, a device can be rated by commercial, industrial, automotive, extended or military specifications. A designer is responsible for choosing the appropriate specification for a given application.

Note that common low-temperature ratings are based on manufacture testing and client needs. A rating below -55 °C is seldom needed and for that reason does not necessarily suggest that a component will fail below this condition. Rather, it was tested down to the lower temperature limit and certified functioning within specification. As a result, components may be able to function at lower temperatures without any detrimental effects. In this case, it is the designer’s responsibility to test and qualify the device for use.

- **“Electrostatic voltage tolerance”**. Electrostatic discharge is one of the most common electronic killers. Most CMOS technologies rate their device to be able to tolerate a certain amount of static discharge.

Other than the device ratings, a component’s behavioural characteristics may be expressed as following specifications:

- **“Operating power”**. All devices need energy to function; therefore current must be sourced to the device. For complex devices, commonly described power uses are related
to active device functions. Power may also be proportional to other operational conditions, such as voltage, operating frequency and temperature.

- “Response times”: Any system expresses time lags and transient responses to input and output functions. These responses are generally proportional to operating voltage and temperature, and are typically expressed by rise and fall times.
- “Efficiency”: This rating is ordinarily associated with power electronics. It stipulates the amount of energy that may be wasted by the device. In some cases this value is also related to the thermal energy generated by the device, and consequently specifies required heat dissipation.

4.3.2 Low-temperature physical effects

To better understand some the specifications, low-temperature effects will be addressed. Each type of component may be influenced by temperature differently, and so the following components and materials, as discussed in the “Arctic Design Guide” [31], will be reviewed.

Metals

The temperature effect on metals is defined by the two characteristics shown by Figure 4-9.

- “Yield strength” which is the point at which a metal starts to deform (strain) under stress, also known as the elastic limit. Force applied to a metal will stretch it elastically until the yield strength. As the stress exceeds this limit, the metal starts to lengthen permanently, changing its strength up to point of failure.
- “Ultimate tensile strength” is the maximum stress than can be applied to the metal, before it starts to lose strength. It is characterized by the point that necking occurs, a narrowing effect indicating reduced tensile strength, and followed by failure.

\[
\text{Stress} \quad \text{Strength} \quad \text{Necking} \quad \text{Yield Strength} \quad \text{Ultimate} \quad \text{Failure}
\]

\[
\text{Strain} \quad \text{Strength} \quad \text{Necking} \quad \text{Yield Strength} \quad \text{Ultimate} \quad \text{Failure}
\]

**Figure 4-9 Typical stress strain curve of a metal**

Temperature influences both yield and ultimate strength respectively, each increasing with reduced temperature. Yield strength tends to increase faster than ultimate strength; therefore, given a large enough rate of change, a situation arises where the two strengths cross. This
indicates the transition from a ductile to brittle material; also known as the brittleness transition temperature [31]. At this temperature a material will fracture before yielding, leading to unexpected failures.

Whether electronic enclosures or the electronic components, low-temperature material selection is critical to a design. For any metal used, the Ductile-Brittle Transition effect must be considered, or the component will be unable to handle low-temperature impact stresses.

**Plastics**

Plastics are used for both structural and electrical insulation applications. Thus there is a need to study additional relevant properties.

- **“Strength”**. Plastics exhibit the same behaviour as that of metals, although the ductile-brittle transition tends to be more gradual and occurring at a much higher temperature than that of metal. Plastics, resins and rubbers tend to be more brittle, with lower flexibility. Table 4-5 shows common plastics with corresponding brittleness transition temperatures.

<table>
<thead>
<tr>
<th>Polymer Type</th>
<th>Britteness temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PS</td>
<td>90</td>
</tr>
<tr>
<td>PVC</td>
<td>-20</td>
</tr>
<tr>
<td>ABS</td>
<td>-25</td>
</tr>
<tr>
<td>PET</td>
<td>-40</td>
</tr>
<tr>
<td>HDPE</td>
<td>-70</td>
</tr>
<tr>
<td>PC</td>
<td>-200</td>
</tr>
</tbody>
</table>

Table 4-5 Ductile-brittle transition of common polymers

Other than the Ductile-Brittle Transition, the following plastic characteristics are also influenced by lower temperatures:

- **“Absorption ability”**. Plastics have a degree of moisture absorption ability. Absorbed moisture contributes to the ductility of plastic. Cold, low humidity environments reduce the moisture content within the plastic, consequently lowering the ductility of the plastic.

- **“Thermal expansion”**. The change in material dimensions combined with brittleness may lead to failure. Therefore plastic and metal combinations need to be carefully selected, to make sure the difference in thermal expansions does not exceed the tensile strength.

- **“Electrical”**. The temperature effect on electrical insulation values is minimal. The main property of interest is the elastic property of wire insulation that becomes rigid and unmanageable.

Plastics are affected similarly to metals, becoming more brittle at cold temperatures. Accordingly, the Ductile-Brittle Transition property should be a prime consideration when using plastics.
Insulated wires

Wire insulation consists primarily of plastic materials susceptible to reduced flexibility and brittleness at low temperatures. The following table shows commonly used insulation materials, with regard to operating temperatures.

<table>
<thead>
<tr>
<th>Flexibility</th>
<th>Insulation compounds</th>
<th>Service temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Other</td>
<td>Neoprene</td>
<td>-20</td>
</tr>
<tr>
<td>Poor</td>
<td>PVC</td>
<td>-20</td>
</tr>
<tr>
<td>Great</td>
<td>Cellular polypropylene</td>
<td>-40</td>
</tr>
<tr>
<td></td>
<td>Polypropylene</td>
<td>-40</td>
</tr>
<tr>
<td></td>
<td>Low-density polyethylene</td>
<td>-60</td>
</tr>
<tr>
<td></td>
<td>High-density polyethylene</td>
<td>-60</td>
</tr>
<tr>
<td></td>
<td>Cellular polyethylene</td>
<td>-60</td>
</tr>
<tr>
<td></td>
<td>Teflon</td>
<td>-70</td>
</tr>
<tr>
<td>Excellent</td>
<td>Silicone</td>
<td>-80</td>
</tr>
</tbody>
</table>

It is clear that Silicone- and Teflon-based insulated wiring should be used at low temperatures.

IC package

An integrated circuit (IC) is made up of multiple sub-components and therefore multiple types of materials such as epoxy moulding compound, a lead frame, internal attachment wires and the diced silicon wafer “DIE”. The temperature-related failure of an IC is due to differences in sub-component rates of thermal expansion.

The thermal expansion coefficient (CTE) reflects the volume changes a material undergoes relative to its temperature. Given a sufficient temperature change, the difference in thermal expansions of individual sub-components will lead to inter-component strain. Combined with brittleness, these strained interfaces may fail. Thus, the main temperature effect on the IC package is thermal deformation as a result of expansion.

![Figure 4-10 IC casing structure](image_url)

There are commonly two temperature ratings given: case operating temperature and component storage temperature. These discrete values are based on the fact that an operating component
versus a cold shelved component undergoes self-heating, causing thermal differences within the component, adding to the internal stresses.

Thus for low-temperature design, it is important to select appropriately rated components.

**Circuit boards**

PCBs are arrangements of wiring, placed on an electrically non-conductive base, the laminate. Some of the most common board materials include: phenolic, paper-filled phenolic resin, glass epoxy, ceramic and polytetrafluoroethylene (PTFE) laminates. Each manufacturer has its own specific process which determines the characteristics of a laminate. What should be important while selecting a PCB is the CTE (coefficient of thermal expansion).

PCB laminate material tends to expand or contract depending on its temperature, leading to stresses on components known as thermal shock. Large PCBs show pronounced bending and curling whilst under extremes temperatures. The warping board causes solder attachment strain, leading to dry joint formation. Figure 4-11 illustrates PCB-IC solder strain as a result of CTE differences.

![Figure 4-11 Thermal expansion effect on a circuit board](image-url)
The corresponding CTEs for common materials used in PCB manufacturing are shown in Table 4-7.

<table>
<thead>
<tr>
<th>Material</th>
<th>Coefficient of thermal expansion $m \times 10^{-6} \cdot \text{m}^{-1} \cdot \text{K}^{-1}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Glass Epoxy Resin</td>
<td>0.14</td>
</tr>
<tr>
<td>FR 4 x -axis</td>
<td>0.12</td>
</tr>
<tr>
<td>FR 4 y -axis</td>
<td>0.70</td>
</tr>
<tr>
<td>FR 4 z -axis</td>
<td>0.14</td>
</tr>
<tr>
<td>Copper</td>
<td>16.0</td>
</tr>
<tr>
<td>Gold</td>
<td>13.5</td>
</tr>
<tr>
<td>Aluminium</td>
<td>23.6</td>
</tr>
<tr>
<td>Lead</td>
<td>29.0</td>
</tr>
<tr>
<td>Solder (60/40)</td>
<td>24.0</td>
</tr>
<tr>
<td>Nylon</td>
<td>80–90</td>
</tr>
<tr>
<td>Epoxy resin</td>
<td>26</td>
</tr>
<tr>
<td>Silicon chip</td>
<td>1-6</td>
</tr>
</tbody>
</table>

Therefore, proper selection of PCB laminate and PCB trace/plating material should be made. Keeping the board relatively small will limit the total extent of thermal expansion.

**Solder**

Under thermal stresses, solder is one of the main structures that fail within PCB design. The main reason for failure is the ductile-brittle characteristics of the solder material. The PCB joint stress is caused by different CTEs; however, failure is caused by insufficient ductility.

Before tensile strength is considered, it is important to understand the types of soldering joint failures. There are three types of failures shown in Figure 4-12:

- “**Pad lift**”. This is common to low quality PCBs. Separation occurs as the conductive layer adhesive fails. This may also be caused by inadequate soldering, where the pad was heated too long, reducing the adhesion to the PCB laminate.

- “**Brittle interface failure**” is when the solder detaches from the copper pad and forms what is commonly known as a dry joint. This may be as a result of cold-temperature brittleness or inadequate soldering.

- “**Docile bulk solder failure**” is where solder undergoes stresses exceeding the ultimate tensile strength. Elongation and then necking occurs, followed by failure. This failure is common to high-temperature electronics.
Because CTE stresses are to be expected, solder should be chosen with very low ductile-brittle transition temperatures. The ductile-brittle transition temperatures of common soldering alloys are shown below:

Table 4-8 Transition temperatures of the studied solders [32]

<table>
<thead>
<tr>
<th>Solder</th>
<th>Transition temperature (°C)</th>
<th>Safe above (°C)</th>
<th>Transition type</th>
</tr>
</thead>
<tbody>
<tr>
<td>99%Sn</td>
<td>-125</td>
<td>-120</td>
<td>Sharp</td>
</tr>
<tr>
<td>Sn-0.7%Cu</td>
<td>-130</td>
<td>-120</td>
<td>Sharp</td>
</tr>
<tr>
<td>Sn-0.7%Cu(Ni)</td>
<td>-130</td>
<td>-120</td>
<td>Sharp</td>
</tr>
<tr>
<td>Sn-37%Pb</td>
<td>-50</td>
<td>-25</td>
<td>Gradual</td>
</tr>
<tr>
<td>Sn-3%Ag-0.5%Cu</td>
<td>-78</td>
<td>-70</td>
<td>Sharp</td>
</tr>
<tr>
<td>Sn-4%Ag-0.5%Cu</td>
<td>-60</td>
<td>-45</td>
<td>Sharp</td>
</tr>
<tr>
<td>Sn-5%Ag</td>
<td>-45</td>
<td>-30</td>
<td>Sharp</td>
</tr>
</tbody>
</table>

It is clear that lead-based solders show the worst behaviour at low temperatures. 99 % Sn solder, on the other hand, can be used down to cryogenic temperatures. Therefore, low-temperature effects can be reduced by using the correct solder compound combined with high-quality PCBs.

**Resistors**

A resistor is a commercial-off-the-shelf (COTS) passive component, used to limit the flow of current when voltage is being applied across its terminals. All resistors are affected by temperature and can be expressed by either a positive or negative temperature coefficient resistance (TCR). The following table shows the TCR for common resistor types, expressed in parts per million per degree Celsius (ppm / °C).
Table 4-9 Resistor TCR values [33]

<table>
<thead>
<tr>
<th>Resistor type</th>
<th>TCR ppm / °C</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>min</td>
</tr>
<tr>
<td>Metal film</td>
<td>+50</td>
</tr>
<tr>
<td>Carbon composition</td>
<td>+500</td>
</tr>
<tr>
<td>Wire wound</td>
<td>+200</td>
</tr>
<tr>
<td>Thick film</td>
<td>+20</td>
</tr>
<tr>
<td>Thin film</td>
<td>+20</td>
</tr>
<tr>
<td>Base diffused</td>
<td>+1500</td>
</tr>
<tr>
<td>Emitter diffused</td>
<td>+600</td>
</tr>
<tr>
<td>Ion implanted</td>
<td>±100</td>
</tr>
</tbody>
</table>

Low-temperature designs would ideally use a resistor with the least temperature dependence, thus allowing for stability over wide temperature ranges. Knowing the resistor TCR values allows designing for a specific operating temperature. Accordingly, thin-film resistors are shown to be the best option for low-temperatures designs.

Semiconductors

Semiconductors are interface devices with adjustable conductivity. By infusing or doping the material with impurity atoms, the electrical conduction within the material can be controlled via a voltage. When positive charge carrier atoms are added to the material, it is called a p-type and when negative free electrons are added, an n-type semiconductor. A PN junction interface is the fundamental building block of both transistor and diode technologies. Semiconductor components function primarily by controlling the flow of current, exhibiting a current/voltage relationship. Consequently the temperature-related effects are visible in the forward-voltage drop and the collector reverse leakage current.

The forward-voltage is inversely proportional to the transistor temperature. As shown in Figure 4-13, decreasing temperature increases the voltage by ~2 to 3 mV / °C. This presents potential problems within precision low-voltage circuitry and may require compensation techniques to mitigate this effect.
The second effect is that of reverse leakage current, which is directly proportional to temperature; thus leakage-current is reduced at lower temperatures, lowering the power consumption of a semiconductor. This is a beneficial effect, therefore not needing any design considerations.

**Photovoltaic cells**

Photovoltaic (PV) cells, commonly known as solar cells, have voltage responses similar to that of semiconductors; consequently temperature affects the cell voltage. The solar cell voltage increases at lower temperatures. Figure 4-14 shows this increase and consequently an increased PV system efficiency.

Temperature dependence is characterized by the temperature coefficient (TC), measured in percentage of nominal voltage per degree Celsius (% / °C).
Solar cells therefore have favourable response to lower temperatures. What should, however, be considered is the open-circuit voltage at a specific low temperature. Neglecting this may lead to values that exceed a system’s maximum input voltages tolerance.

**Crystals**

Crystals are piezoelectric material resonating devices used for generating precise frequencies. Most electronic devices make use of these crystals to generate accurate clock signals, ideal for timing critical functions. Resonance is achieved when voltage is applied to the crystal, subsequently deforming the crystal; as the voltage is removed the structure reverts to its original shape, creating an inductive voltage response. Therefore, resonance is based on physical structure and crystal cut.

The crystal structure is affected by both temperature and age, and these therefore affect frequency. Aging is the gradual change of a crystal’s fundamental frequency over time. Whereas temperature dependence is expressed by the crystal temperature coefficient, the rate of frequency changes per degree Celsius. Typical temperature coefficients range from ± 60 to ± 3 ppm/ °C. Although these coefficients are proportional to temperature, most crystals have at least one temperature at which this coefficient is zero.

The importance of frequency stability is due the fact that frequency shifts may render equipment unusable, or in the case of clock functions will introduce large accumulative timing error. Additionally, mechanical stresses such as the thermal expansion of the crystal housings and PCBs deform the crystal structure and give rise to additional frequency changes.

To reduce these effects, crystals are manufactured in temperature-compensated and temperature-controlled versions, making use of specific cuts to reduce the frequency effects.

Therefore, low-temperature crystals should be selected with the smallest temperature coefficients.

**Capacitors**

Capacitors are parallel-plate charge storage devices. Two electrical plates are separated by a dielectric medium, storing energy in the form of electric charge. Ideally, the charge is stored permanently, until used. The ability to store charge is measured by capacitance, determined by physical dimensions and the dielectric material used.

Capacitors are typically grouped into dielectric types, with unique temperature, frequency and age sensitivities. The capacitance is mainly influenced by the dielectric medium, which is effected by temperature. The capacitive effect can be expressed by the temperature coefficient capacitance (TCC) as shown in Table 5-11.
Table 4-10 Capacitor temperature coefficients

<table>
<thead>
<tr>
<th>Type</th>
<th>TCC ppm/ °C</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ceramic</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low permittivity</td>
<td>+80</td>
<td>+120</td>
<td></td>
</tr>
<tr>
<td>Medium permittivity</td>
<td>-600</td>
<td>-80</td>
<td></td>
</tr>
<tr>
<td>Film capacitors</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Polypropylene</td>
<td>-200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Polystyrene</td>
<td>-100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mica</td>
<td>-200</td>
<td>+200</td>
<td></td>
</tr>
<tr>
<td>Tantalum</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pellet</td>
<td>+100</td>
<td>+200</td>
<td></td>
</tr>
<tr>
<td>Foil</td>
<td>+500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electrolytic</td>
<td></td>
<td>±1000</td>
<td>±2000</td>
</tr>
</tbody>
</table>

Used as charge reservoirs, capacitor variation can be easily be neglected. Nonetheless filter designs shows significant frequency response due to fluctuating temperatures.

Therefore, a design should consider the TCC value. Reducing the temperature effect can be achieved by either selecting a capacitor with minimal TCC or using compensation techniques where both positive and negative TCC components are used.

**Inductors**

An inductor is a wire-wound coil surrounding a core consisting of either air or metal ferrite. Metallic core coils experience small inductance changes due to temperature. Thermal expansion of the coil and core lead to small dimensional changes affecting the inductance value. Moreover metal magnetic coupling is also affected by temperature, therefore effecting efficiency. Air-core, inductors are not as easily affected by thermal expansion and show no significant temperatures effects [31].

The complex nature of individual inductors makes this a difficult effect to quantify; dependencies are unique to each individual manufacturer’s component. Selection of low-temperature inductors would therefore be based on each component’s rating and specific application.

**Liquid crystal displays**

Liquid Crystal Displays (LCDs) are used for common electronic displays. LCDs use liquid crystal molecules between two electrodes, combined with perpendicular polarized filters to polarize light. Subsequently, light passing through the LCD can be either passed or blocked. At lower temperatures the rotational viscosity of polarizing crystal decreases. Common LCDs are rated to function from -20 to 65 °C, with temperature affecting the LCD response time. With the exception of some industrial LCDs, displays are not suited for extreme cold. It is also seldom required to have a display in an environment where no human operator goes. Thus for
a low-temperature design, the question whether a display is practical and necessary should be evaluated.

**Integrated circuits**

Digital logic Integrated Circuits (ICs) are primarily made up of integrated transistors, encapsulated within a mechanical structure. Both of these have already been discussed.

The only effect that has yet to be mentioned is the transition of digital logic. The temperature effects of the majority of digital ICs are based on gate turn-on and turn-off times. Decreasing temperature slows down a circuit response. Additionally, the gate threshold voltages may change, making low-voltage circuits more prone to errors.

**Filters**

Electronic analogue filters are circuits designed to either attenuate or pass specific bands of frequencies. These circuits are made up of discrete components comprising of resistors, capacitors, inductors and transistors. All of these components contribute to the frequency response of a filter and depending on the design, may require precise values, making the filter sensitive to variations. Thus temperature may affect the filter response as a result of sub-component sensitivities. A designer has a responsibility to identify the components with the most temperature dependence and correspondingly design a circuit to minimize these effects. Therefore, a balance between design sensitivity and component stability has to be achieved.

**4.3.3 Design method**

To design for low temperatures, a few strategies are available. The challenge is to find low-temperature components in an industry that only supports temperatures down to -55 °C; and in the case where components cannot be found, the challenge is to mitigate the environmental effects.

**Preferred available parts**

The first level of a low-temperature design:

1. Identify the component level requirements, needs, specifications and functions;
2. Compile a list of available components. Therefore, find state-of-the-art components and establish a database of low-temperature components;
3. Allocate available components to functions, stipulating their specifications:
   a. With multiple component options; compare specifications and cost;
   b. Reduce component allocation to a list of preferred parts;
4. Identify all the functions and specifications that cannot be allocated to an available component resource. From this list, identify a list of component that come close to requirements:
a. Identify shortfalls;
b. Mitigate effects either in design or alternative component options;
c. Stipulate unreachable design goals;

5. In case of components that do not meet the specifications, a component may be considered for use outside its rating. However, it is the designer’s responsibility to qualify the component within an experimental setup, and to validate and consequently create new specifications.

For the purpose of this research, rated by the level of importance, the primary specifications will be evaluated:

![Component availability hierarchy](Image)

**Figure 4-15 Specification hierarchy**

**Protective architecture**

Protective architecture is the process of mitigating extreme conditions that may lead to reduced systems reliability. Protection architecture acts to detect conditions and faults that may lead to failure, after which it attempts to prevent the fault-causing failure. By reducing the number of faults, the overall system reliability can be enhanced [33].

Thus it can be categories into two types:

1. “Prevention”, i.e. remove the condition that may lead to failure and damage:
   - Under-voltage detection and brown-out shutdown;
   - Shutting down overheating systems.

2. “Mitigation”, i.e. when a fault has occurred, damage is minimized by isolating the fault or removing conditions that may lead to further damage, thus protecting the system against secondary faults:
   - Isolating shorts circuits. This protects against catastrophic damage, thus total system failure is averted by isolating the fault or shutting down the system.

In the case of this research, the primary condition that may lead to complete systems failure is that of extreme low temperature. Although this would come at the cost of operational time, the systems could potentially be shut down to prevent damage in extreme conditions, and be reactivated when the conditions have passed.
4.4 Low-power design

The objective of low-power design is to reduce the overall power consumption of an electronic system. Within portable systems, energy is a limited resource; by improving a system’s efficiency one can reduce the energy consumption and consequently the overall cost of the system. Electric power $P$ is defined as the rate of energy used within an electric circuit, expressed by:

$$ P = V \times I, \quad (4.13) $$

where $P$ = the electric power, $V$ = load voltage, and $I$ = current flow.

Any and all work done by any electric system is eventually converted into another form of energy such as radiation, heat or movement. In terms of an electronic system, energy converted either works, or is wasted by the inefficient use of power.

The relationship between the two is also known as the system efficiency. An ideal system would have an efficiency of 100 %, but within any real-world application this is never the case. Thus there will always be a measure of loss within a system. A designer strives to minimize these system losses, by identifying the loss mechanisms within a circuit.

The main design constraint within portable designs, especially embedded designs, is the relationship between performance, power-consumption and power-availability. It is by measuring the use of active processes, knowing where power is allocated to, that power can be budgeted and consequently improvements made.

For this reason, power dissipation within electronic components will be reviewed next. To simplify the deduction, low-power design will be discussed first in terms of hardware, followed by software design.

4.4.1 Low-power hardware design

At a hardware level, all electronic systems consist of sub-components, either as discrete or integrated circuits, and their use of energy is grouped into two distinct types:

"Static power", which is the use of power in the form of:

- Quiescent operation bias currents;
- Load currents;
- Non-ideal components leakage currents [35].

"Dynamic power" is power consumption as a result of switching circuitry and dissipating power through the charge and discharge of reactive loads. Dynamic power makes up 85 -90 % of power consumption within a digital design and is therefore the primary form/mechanism of energy consumption.
Resistors

Resistors are the most fundamental component within an electric circuit, and can be described as devices that inhibit the flow of current: energy is converted directly into heat. Almost all forms of power dissipation can eventually be described by an equivalent resistive circuit.

Resistance is expressed by “Ohm’s law”:

\[ R = \frac{V}{I}, \]  

(4.14)

where \( R \) = resistance, \( V \) = voltage applied, and \( I \) = current flowing through the resistor.

Combining this with the electric power relationship (4.13) yields the power consumption \( P_L \) of a resistive load \( R \), shown in terms of applied voltage \( V \):

\[ P_L = \frac{V^2}{R}. \]  

(4.15)

Thus power within a resistor can be reduced by increasing the impedance or, alternatively, reducing the applied voltage.

Capacitors

The second most common components within electronic designs are capacitors. Analog designs make use of the frequency dependence of these components to attenuate or pass signals. However, within digital designs, this parallel plate component is primarily used as a charge reservoir, storing and releasing electric charge with switching operations. It is because of this active switching that capacitors not only consume power in static manner, but also dynamically.

**Capacitor static power**

Static power use is a result of the internal capacitor leakage current. All capacitors make use of dielectric material to electrically separate their parallel plate interfaces. This dielectric material is far from an ideal insulator; it therefore allows small amounts of current to leak and can be described by an equivalent series resistance ESR, as shown in Figure 4-10.

![Figure 4-16. Capacitor ESR](image)
Each type of capacitor technology uses different dielectric materials, consequently exhibiting unique leakage currents. The four most common types of capacitor with their respective leakages are show in Table 4-11.

<table>
<thead>
<tr>
<th>Type</th>
<th>Typical Leakage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Film</td>
<td>5 nA</td>
</tr>
<tr>
<td>Ceramics</td>
<td>20 nA</td>
</tr>
<tr>
<td>Tantalums</td>
<td>1 µA</td>
</tr>
<tr>
<td>Electrolytic</td>
<td>5 µA</td>
</tr>
</tbody>
</table>

*Capacitor dynamic power*

Dynamic power is the process of charging, and the power consumed is shown by:

\[
P_{cap} = CV^2 f, \tag{4.16}
\]

where \( P = \) power consumed,
\( C = \) capacitance,
\( V = \) voltage applied, and
\( f = \) switching frequency.

Dynamic power can therefore be limited by reducing any one of the capacitance, voltage or switching frequency. Thus, optimisation would first start with technology: appropriate component selection, and secondly by selecting the appropriate operating conditions.

*Inductors*

The second energy reservoir device is that of inductors, using magnetic fields to store and release energy.

*Inductor static power losses*

Static power loss is as a result of the internal wire resistance. As defined by “Ohm’s law”, current flowing through a resistive load will exhibit a voltage drop, therefore power will be consumed and converted into heat.

Specific inductance is determined by coil length, wire gauge, inductor dimensions and inductor core material. The wire will therefore exhibit a resistive property that is a function of its length.

Copper wire has a resistivity \( \rho = 1.724 \times 10^{-8} \Omega \cdot \text{m} \) at 20 °C and in the case of smaller inductors, where typically thinner wire is used, they exhibit higher resistances. Thus the resistance for a specific length of wire with a known diameter can be shown to be:

\[
R = \rho \cdot \frac{L}{A}, \tag{4.17}
\]

where \( R = \) resistance,
$L$=length, and
$A$=cross section area.

Figure 4-17, shows the equivalent series resistance of an inductor:

![Figure 4-17 Non ideal inductor](image)

When referring to “dynamic power loss”, the term is commonly associated with digital switching circuits. Therefore in the case of analogue inductor loss, the term “switching loss” is used to avoid confusion.

**Switching power loss**

This is a frequency-dependent loss. Inductors are primarily used within power-switching applications and loss is measured by the variation of magnetic energy contributed by an inductor compared to the magnetic energy released [36].

1. **Skin effect loss** within a conductor when high frequency signals are applied: resistive eddy currents form within the conductor, opposing the AC flux, consequently increasing the resistance;
2. **Hysteresis loss**: this pertains where magnetic core inductors are used. As with all magnetic cores, inductors create magnetic fields focussed within the core. The core initially resists magnetization, expending energy in the form of heat; this process can be simply considered as magnetic friction. This property is determined by the frequency dependent permeability of the core material;
3. **Eddy currents loss** is when small localized magnetically induced currents are introduced within the inductor core. These currents create impeding magnetic flux, hindering the transition of magnetic fields. Separating the core material with laminated dividers can reduce these currents.

Similar to the low-temperature design criteria, low-power inductor design is highly dependent on the application and the manufacturing specification. Therefore, appropriate component selection is vital for efficient design.

**Diodes**

Diodes are semiconductors using a PN junction interface to limit the directional flow of current. Whilst in forward conduction, a voltage drop is created across the junction. Depending on the technology and active current, voltage drops can range between 0.3 and 0.8 V. A diode can therefore conduct large amounts of current whilst maintaining a relatively fixed voltage. Thus the power can be shown to be proportional to the conduction current:
\[ P_D = V_D \times I = 0.8 \times I, \]

where \( V_D \) = voltage drop (~0.8 V), and 
\( I \) = current.

Limiting the use of diodes within a design would therefore reduce losses. In the case where diodes are used, lower voltage small-signal diodes are available that have lower threshold voltages.

**Transistors**

_Bipolar junction transistors_ (BJTs) are current-driven amplifiers, where amplification can be achieved by applying a small base current to a controlling terminal of the transistor. Power is consumed by this control current \( I_b \), dissipated internally, and shown as an input resistance \( R_{be} \). As shown in the figure the BJT operates as a current-controlled current source.

![BJT internal resistance illustration](image)

**Figure 4-18 BJT internal resistance illustration**

Field Effect Transistors (FET) are voltage-controlled semiconductor amplifiers. Most digital integrated circuits make use of metal oxide semiconductor FETs, also commonly known as MOSFETs. The controlling gate terminal of a FET resembles a capacitor, using metal oxide as a dielectric medium.

**Gate-leakage**

FET static loss is attributed to the gate-leakage, therefore determined by dielectric thickness and feature size.

With FET manufacturing, the feature size plays a huge role in transistor power consumption. Following Moore’s Law, manufacturers continually improve transistor fabrication technology, therefore making FETs smaller, faster and consequently denser per surface area. Reducing the feature size decreases the transistor’s threshold voltage, allowing digital application to function at reduced operating voltages.

Although this reduces the circuit’s dynamic power loss, it unfortunately leads to reduced gate impedance, consequently increasing the leakage.
Sub-threshold leakage

Along with gate-leakage, when feature sizes start ranging in nanometers, a second type of leakage begins to take effect. Sub-threshold leakage is triggered by the reduced threshold limit, causing current to flow between the source and drain terminals, whilst in an off state.

Leakage power ($P_L$)

This is the power loss due to transistor technology being powered-on dissipating a small amount of power. For low-power applications, the power consumption of FETs is superior to that of a BJT equivalent.

Integrated circuits are lumped semiconductor circuits, assembled onto a silicon substrate, the dominant semiconductors being transistors. The ICs are therefore subject to the same losses as the transistor technology used in their design. As a result, low-power components are mostly fabricated using complementary pairs of MOSFET transistors, also known as complementary-symmetry metal–oxide–semiconductor (CMOS) technology.

Logic circuits make use of CMOS transistors to perform tasks. Thus power is consumed in a quiescent state, where the logic is not performing any task, hence no charge or discharge is involved.

Power is consumed primarily whilst performing logic tasks, thus as transistors are actively changing states. Power is therefore a function of switching activity. Circuit complexity and layout also contribute to the power use. The figure shows the three types of digital logic power loss.

![Figure 4-19 Dynamic charge current [37]](image)

Switching power ($P_{SW}$) loss

Switching power loss is defined as power loss due to state changes of the gate. The output capacitance $C_{eff}$ is charged or is discharged, consuming power. Therefore Switching Power can be shown to be:
\[ P_{sw} = \frac{1}{2} \times C_{eff} \times V^2 \times f_{clk} \times \alpha, \]  

(4.18)

where  \( P_{sw} \) = power consumed as a result of switching,
\( C_{eff} \) = is the effective load capacitance,
\( V \) = the circuit operating voltage,
\( f_{clk} \) = is the operating frequency of the circuit, and
\( \alpha \) = the switch activity weighting factor, defined as the probability a gate will change states [38].

\textit{Short-circuit power (}\( P_{SC} \textit{)}

This is power loss due to the short-circuit path between rails, whilst a transistor is switching. This crowbar-action is responsible for approximately 10-15% of the dynamic current. The total power consumed by a logic gate \( P_{LG} \), can be expressed by:

\[ P_{LG} = P_{SW} + P_{SC} + P_L. \]  

(4.19)

\textbf{Bias circuits}

One of the most common uses for resistors within digital circuits is for Pull-up resistors. A good design uses large resistor values, to reduce the switching current within these resistors and to minimize port leakage current.

\textbf{Controllers}

The heart of any digital data acquisition system is the controller unit. This can be either a micro controller unit (MCU) or a microprocessor unit (MPU). For this project the choice between the two is based on power consumption, complexity, cost and product support. MCUs are single-chip mini computers, including all the on-chip resources needed to function autonomously. MCUs typically have faster boot times, relatively low component and development cost and are extremely low power consumers.
In contrast MPUs are general-purpose digital computer processors, requiring external circuitry to function as full-fledged computers. The complexity, layout, cost and the knowledge requirements for MPU designs make them ill-suited for relatively simple autonomous data acquisition systems. The following sections will therefore specifically focus on MCU technology and constraints.

*Operating voltage*

MCUs consist primarily of transistors and capacitors. As discussed in the previous section, whether static or dynamic, power consumption is proportional to the supply of voltage. In an effort to reduce the dynamic power consumption, advances in technology have reduced transistor feature sizes down to 90 nm. As a result, core voltages have dropped from 3.0 V down to 1.2 V, effectively reducing dynamic power. However, as was shown in the discussion on MOSFETs, decreasing the feature size introduces additional leakage currents. The following table compares leakage with dynamic power, based on feature sizes:

**Table 4-12 MCU process technology [39]**

<table>
<thead>
<tr>
<th>Process technology (µm)</th>
<th>Leakage power (Normalized)</th>
<th>Dynamic power (Normalized)</th>
<th>Core voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35</td>
<td>0.5</td>
<td>2.8</td>
<td>3.0</td>
</tr>
<tr>
<td>0.25</td>
<td>0.75</td>
<td>2.0</td>
<td>2.5</td>
</tr>
<tr>
<td>0.18</td>
<td>1.0</td>
<td>1.0</td>
<td>1.8</td>
</tr>
<tr>
<td>0.130</td>
<td>1.5</td>
<td>0.75</td>
<td>1.5</td>
</tr>
<tr>
<td>0.090</td>
<td>2.0</td>
<td>0.44</td>
<td>1.2</td>
</tr>
</tbody>
</table>

It is shown that at 0.18 µm, the primary power loss mechanism changes from dynamic to static leakage. The selection of appropriate technology is therefore the trade-off between performance and power consumption within the embedded system.

![Figure 4-21 Process technology dynamic-static power [39]](image)
Because most low power applications spend 99% of operating time in idle state, low-power MCUs are commonly manufactured within the range of 25-35 $\mu$m.

**Clock sources**

CPUs also come with different clocking schemes. The type of clock will fundamentally determine the power consumption of the systems. Additionally, MCUs commonly provide a means to switch between clocks, depending on the computational needs. The common clock sources for an MCU are shown in the table:

<table>
<thead>
<tr>
<th>Oscillator</th>
<th>Frequency</th>
<th>Start time (µs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Internal fast RC</td>
<td>8 MHz</td>
<td>0.001-0.010</td>
</tr>
<tr>
<td>Low-power RC</td>
<td>31 kHz</td>
<td>0.3</td>
</tr>
<tr>
<td>Primary crystal</td>
<td>8 MHz</td>
<td>0.5-1.0</td>
</tr>
<tr>
<td>Internal RC + PLL</td>
<td>32 MHz (8 MHz x 4)</td>
<td>1.0</td>
</tr>
<tr>
<td>Primary crystal + PLL</td>
<td>32 MHz (8 MHz x 4)</td>
<td>1.5-2.0</td>
</tr>
<tr>
<td>Secondary crystal</td>
<td>32.768 kHz</td>
<td>100-1 000</td>
</tr>
</tbody>
</table>

Of all the clocking systems, the internal Low-Power RC clock is considered to be the clock requiring the least amount of power. The only drawback in using the RC oscillator is stability. A crystal oscillator has far superior stability.

Once again, the application will dictate the choice in clocking scheme.

**External connections**

An MCU does not function in isolation; therefore it must interface with the outside world via input/output (I/O) ports. These I/Os come in both analogue and digital interfaces, used for communication control and measurements.

Analogue input ports have very high input impedances; therefore they consume very little current. The digital I/O pins, on the other hand, are perhaps the most overlooked peripheral function on an MCU. For every transition of a digital logic gate, the change of state consumes power. Unused digital I/O pins, which are left floating, may be driven by an external noise source, consequently inputs are allowed to possibly drift around the transition threshold, causing high frequency switching and, if left unchecked, can consume up to 100 $\mu$A [39]. Therefore it is recommended to terminate any unused pin with a pull-up resistor or configure the digitally controlled pin as an analogue input.

**Instruction type**

CPUs come in three types of instruction sets: CISC, RISC and ARM. Complex instruction set computing (CISC) uses variable length instructions, which characteristically have a higher code density. They therefore require multiple clock cycles, increasing the overall power consumption.
Reduced instruction set computing (RISC) on the other hand has fixed length instructions. Execution requires only single-clock cycles, using fewer transistors than a CISC machine.

Advanced RISC Machine (ARM) expanded the fixed instructions set with the “Thumb” feature. This allows the CPU to support both 16-bit and 32-bit instructions, consequently improving code density by 30%. Additionally the instruction set has also been expanded to include more complex operations and better memory management.

Both RISC and ARM are close competitors when it comes to power consumption; comparing these is no easy task. Certainly the biggest choice that will influence the design is system performance.

Therefore, the designer must once again assess the requirements versus performance and find a compromise between specifications. Referring back to equation (4.18), it was shown that power consumption is proportional to the activity factor α and the operating frequency. Therefore, computational requirements will dictate activity and consequently energy use.

For a data acquisition unit, the activity factor is expected to be low. Taking the complexity of ARM into account, RISC architecture would therefore be preferred.

**Voltage regulators**

Most circuits require stable power supplies to function. Variation on a supply may cause a system to fail and introduce unwanted noise to a circuit.

Because power is proportional to voltage, it would be ideal to run a circuit at lower voltages. In most cases power supplies such as batteries are only available in fixed values, thus there is a need for voltage scaling.

The simplest power supply would be that of an unregulated supply. This is only possible in cases where the supply is within the needed voltage range. A simple example would be series 1.5 V alkaline battery pack delivering a voltage range of 3.2 to 2.4 V. Where circuitry is sensitive to voltage changes, voltage regulators are needed.

To accomplish stable voltage scaling, either linear voltage regulators or DC to DC converters can be used.

**Linear voltage regulator**

The most inexpensive option is that of a linear voltage regulator. These regulators are transistor current sources, delivering load current at a fixed output voltage. The power consumption of a linear voltage regulator is shown in Figure 4-22 as an equivalent series resistance dissipating the differential excess voltage. Surplus voltage is dissipated and converted to heat.

Their simplicity, low cost, low noise operation and load handling make them the most popular option for small projects.
Figure 4-22 Voltage regulator layouts

However, linear regulators have three major drawbacks:

1. A linear voltage regulator can only deliver output voltages lower than its input voltage;
2. They are extremely inefficient. The step-down efficiency is equal to the output/input voltage ratio. Therefore, a lot of energy is wasted;
3. Because of the high energy wastage, the common linear regulator requires a heat sink to dissipate excess heat.

Switch-mode regulator

On the other hand, switch-mode regulators make use of current switching, as shown in Figure 4-24, to convert a voltage to appropriate levels.

Through switching, a capacitor is allowed to charge and discharge around the desired voltage. Current is thus used on demand, not shunted through a resistor. Losses are only attributed to the internal current source resistance. Other than a linear regulator, almost all the energy is transferred effectively.

Based on an inductor switch-mode DC/DC converter, the following figure illustrates the switching process.
Switch mode losses are due to the following effects:
- Diode voltage drop (Schottky diode, usually 0.4 V – 0.8 V);
- MOSFET losses;
- Inductor losses;
- Capacitor equivalent series resistance.

Common low-power switch mode regulators can achieve up to 95% efficiency. The switch mode efficiency $\eta$ can be found using the relation:

$$V_{sys}I_{sys} = \eta V_{bat}I_{bat},$$

(4.20)

where $V_{sys} =$ system require voltage,

$V_{bat} =$ the battery input voltage,

$I_{sys} =$ the system load current, and

$I_{bat} =$ the battery input current.

Most switching supplies are designed taking the following into account:

- Input voltage range;
- Output voltage;
- Maximum output current;
- Optimum efficiency.
The efficiency is shown to be a function of input voltage and output current. Therefore, choosing an appropriate regulator type must be done to optimize for maximum efficiency. It is also clear that buck converters tend to be more efficient than boost converters, operating at a wider load range than boost converters with a narrow field of load efficiency.

4.4.2 Low-power software design

This section focuses on MCU power saving strategies. Because MCUs are the core of an imbedded system, they tend to be the main power consumers. Therefore design trade-offs need to be made. One of the main consumers of MCU power is that of dynamic switching, as shown in Section 4.4.1. This is a function of operating frequency. The focus of low-power firmware is to manage performance, execution speed and power consumption.

Systems performance scaling

The power use within an MCU cannot be quantified in terms of a single fixed and documented value. Power is rather expressed as a function of a certain operating conditions, specified as supply voltages, clocking frequencies and active peripherals modules.

To reduce frequency-related power consumption, two options are available: either stop the system or slow it down. The latter is called frequency scaling and this can be applied either to the system core or a selected peripheral function. An MCU shares its system clock between core and peripherals. Each one of these may be selected as a clocking source for the MCU. An internal clock uses less current than external.

Three of the main functional blocks of the system are dependent on these sources, as shown in the following block diagram. Between the MCU core, peripheral functions and the Real-Time Clock and Calendar (RTCC), each can receive its own clocking signal. It is also possible in most cases to multiply and divide the fundamental clock signal to achieve either higher or lower clocking frequencies.

---

**Figure 4-25 Efficiency versus load current curves [40]**

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Manufacturers specify power consumption in terms of µA/MHz or µA/MIPS. By slowing down a CPU by 1/128 of its active clock frequency, power consumption can be reduced by as much as 65%. However, this leads to longer instruction processing times, therefore lowering performance, and reducing the µA/MHz efficiency.

To reduce active power, MCU manufacturers have made certain clock schemes available to designers [41]:

**Active-mode**

Within this mode an MCU is run at its full performance, supporting all the available peripherals. The core and peripheral modules function from the same clocking source.

**Doze-mode**

Internally, the MCU core and peripheral modules have two separated clocking busses. The operating frequency of the MCU clock can therefore be reduced without affecting the peripheral system, thereby allowing a power reduction of as much as 35-75%. By lowering the core execution speed, power and performance are reduced without affecting the timing of critical peripherals.

**Idle-mode**

In this mode, the MCU essentially stops executing instructions while still allowing peripheral modules to continue operating. When in idle-mode the program is stopped and waiting for a wake-up event. This is a convenient mode for situations where processing is only needed in intermittent intervals. While in idle-mode all the peripherals and clocks are available, with the exception of the program counter that is halted. As a result, power consumption can be reduced by up to 75%.
Sleep-mode

In sleep-mode, the primary clock sources, with the exception of the real-time clock and calendar (RTCC), are disabled, consequently disabling any clock dependent functions. Only volatile memory and asynchronous functions are available thereafter. Sleep-mode can reduce power consumption up to 90%.

Deep-sleep mode

Within “shut down”, also referred to as “deep-sleep mode”, power can be reduced by 97%. This mode reduces the current consumption to the lowest level an MCU can sustain without physical switching off. In deep-sleep, all clock function, peripherals and volatile memory are suspended. The only distinguishing difference between deep-sleep-mode and a powered-down device is that an external wake-up source is still available.

By essentially switching off the entire MCU, no lower power mode is available, short of physically removing power. Within this mode the MCU is usually in a state of constant reset, waiting for an external interrupt to release the reset. Depending on the type of MCU, a few registers may be available to save the MCU state before shutdown, allowing the system to distinguish between reset and shutdown.

Clock-switching

Although not part of the operating modes, within multi-clock systems a clock-switching feature is available to developers. This feature allows the MCU to change clock sources dynamically within code and thus allowing the switch between performance and efficient clock frequencies on demand.

Task scheduling

The second step to managing power consumption is to reduce the time the MCU is active, thus avoiding unnecessary activity. Transistor losses are a function of frequency but also proportional to the effective activity weighting factor $\alpha$.

By scheduling the work load, a system devotes only a fraction of its time for computing. The result is a reduced activity factor. By combining this strategy with the appropriate clocking scheme power consumption, dynamic power can be reduced.
The total power consumed for a system performing intermittent tasks can be demonstrated as:

\[ P(t) = \frac{[P_{\text{Active}} \times t_{\text{Active}}] + [P_{\text{Sleep}} \times t_{\text{Sleep}}]}{t_{\text{active}} + t_{\text{sleep}}}, \]  

where \( P(t) \) = total power consumed,
\( P_{\text{Active}} \) = power whilst MCU active,
\( P_{\text{Sleep}} \) = power whilst MCU in sleep,
\( t_{\text{Sleep}} \) = time period MCU in sleep, and
\( t_{\text{Active}} \) = time period MCU active.

Figure 4-27 MCU scheduling power modes [42]

Figure 4-28 Sensor task power consumption
Sub-system partitioning

Partitioning is the scaling of functions within a system. To conserve power, features are disabled while they are not in use.

An MCU is effectively an integrated computer system, built with integral peripheral functions. It is the designer’s responsibility to choose an MCU that has all the necessary features, but also to make sure that the no redundant features.

The table shows common MCU peripheral power requirements:

<table>
<thead>
<tr>
<th>Peripherals</th>
<th>Static</th>
<th>Dynamic (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>785 µA</td>
<td>1000</td>
</tr>
<tr>
<td>UART</td>
<td>NA</td>
<td>200</td>
</tr>
<tr>
<td>SPI</td>
<td>NA</td>
<td>700</td>
</tr>
<tr>
<td>I2C</td>
<td>NA</td>
<td>1000</td>
</tr>
<tr>
<td>Comparator</td>
<td>NA</td>
<td>27</td>
</tr>
<tr>
<td>RTCC</td>
<td>NA</td>
<td>1</td>
</tr>
<tr>
<td>Timers @ 32 kHz</td>
<td>NA</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>@ 16 MHz</td>
<td>150</td>
</tr>
<tr>
<td>WDT</td>
<td>NA</td>
<td>1.5</td>
</tr>
<tr>
<td>Brown-out</td>
<td>6 µA</td>
<td>35 – 50</td>
</tr>
<tr>
<td>Digital input</td>
<td>NA</td>
<td></td>
</tr>
</tbody>
</table>

→ Values based on Pic24FXXX MCU

Thus, if an MCU’s functions power requirements are known, it is possible to calculate the average consumption per module, given that the operation time is predictable.

4.4.3 Micro-power measurement methods

One of the most common current measurement techniques is current shunt measurement. It makes use of a relatively small series resistor to detect current flow. It can be one of two types: a high side current detector connector to VCC and the load, or a low side current detector connected to the load and ground. The figure shows the two types that can be set up.
Whilst this is one of the most common detectors, it does have some limitations. For one, the current detection resistor produces a voltage drop proportional to the current flow. Given a large enough current range this may produce unwanted voltage fluctuation. For that reason, to detect a large current range, a small resistor is needed, and for very low current ranges a sufficiently large resistor is needed. As a result, this method limits the testing to certain current ranges, making it inadequate for applications where dynamic current may be orders of magnitude larger than a system’s static current.

The second method used to detect current is the use of a capacitor discharge circuit, as shown in Figure 5-30 below and given by:

\[ I = C \frac{\Delta V}{t}. \] (4.22)

### 4.5 Energy storage systems

Thus far the main discussion has been on the topic of energy consumption; however, no systems can function without an energy source. As an autonomous data capturing device, the system calls for the use of either an independent or renewable power source. When deciding on the type of energy storage system, the following properties have to be assessed:
- Capacity;
- Power available / instantaneous power capacity;
- Depth of discharge;
- Discharge time;
- Efficiency / internal losses;
- Durability / cycling capacity for renewable systems;
- Cost.

This section focusses on some of the different types of system available.

### 4.5.1 Super capacitor storage

Super Capacitors are similar to normal capacitors, except they have massive storage capacity, making them especially useful for DC applications.

Because there is no electrochemical process involved, capacitors have a low ESR, allowing high charging and cycle rates. This makes super capacitors very durable, in the range of 8–10 years, with efficiencies up to 95% [43].

However, super capacitors have two major drawbacks. Firstly, because of high self-discharge, energy has to be used immediately. Secondly, although super capacitors have huge capacities, this still does not come close to that of chemical batteries.

Therefore, super capacitors can only be used in applications where high bursts of power are required with the infrastructure to recharge between pulses. This makes super capacitors unsuitable for low-power applications.

### 4.5.2 Battery storage

In the “The Handbook of Batteries” [44], a comprehensive description of batteries is discussed, providing the basis for this section. Batteries are electrochemical energy storage units that can deliver electric current. The type of battery can be divided into two sub-categories, namely:

1. **Primary batteries**: this category consists of non-rechargeable batteries capable of delivering power on demand. They typically have higher capacities than their rechargeable counterparts and have a very low self-discharge, giving them long shelf lives;
2. **Secondary batteries**: these are rechargeable batteries that tend to discharge relatively quickly over time, therefore requiring a charge before use. These types of batteries are not suited for long storage, hence they are unsuitable for low-power applications.
Capacity ratings

The first characteristic of a battery is that of capacity. Because batteries are electrochemical cells, different chemistries will deliver distinctive amounts of energy. This capacity is typically described in terms of specific energy, expressed in Wh/kg. Apart from capacity, cells have the ability to deliver instantaneous power, referred to as the battery’s specific power, expressed by a value measured in W/kg. Figure 4-31 shows the relation of these properties to some common battery chemistries.

![Figure 4-31 Energy storage capability of common commercial battery systems [45]](image)

Thus it is important not only to know the energy required by a system, but also the power requirements of its specific application.

Temperature effects

In this research and detector plan, temperature plays an important role throughout the design process, and for batteries this is no exception. Because batteries are based on chemical reactions, it stands to reason that temperature influences the battery performance.

The first effect evident is loss of capacity at lower temperatures. With reduced temperature the nominal cell voltage starts decreasing. Because power (Section 4.4.1) is a function of voltage, both capacity and power availability are reduced with lower voltage. This effect can be seen as a temperature-dependent equivalent series resistance within the battery.

Not only does this affect capacity, but a system may even cease to function when the cell voltage falls below operational requirements.
Lowering the temperature of a battery may also cause physical harm to the battery. Most battery systems make use of an electrolytic fluid, hence are susceptible to freezing. This may result in container damage causing leakage of hazardous chemicals, leading to possible combustion and environmental contamination.

Temperature is a determining factor in battery selection, affecting the reliability and performance. Only through careful consideration of chemistries and the implementation of appropriate design can this effect be mitigated.

**Discharge effects**

A battery’s function is to deliver energy, in the form of current. An ideal power source would deliver 100% of its capacity, irrespective of current and depletion. However, batteries are not ideal power sources, but are affected by internal resistances. Increasing the discharge current rate will therefore cause the terminal voltage to drop proportionally. Batteries with large internal resistances will therefore show poor performance in supplying high current loads.

Batteries can be discharged in the following four manners:

1. *Constant Resistance*: The resistance of the load is kept constant throughout the discharge cycle. As the battery is depleted, the cell voltage decreases, therefore proportionally the load current is decreased;
2. *Constant Current*: The load resistance is scaled proportional to voltage to keep the current constant;
3. *Constant Power*: The current increases during the discharge as the battery voltage decreases, thus discharging the battery at constant power level;
4. *Pulsed Loads*: In the case of switch mode power supplies, a battery is put under pulsed current loads, whereof the frequency and duration of pulses are critical factors effecting capacity. A battery’s capacity is influenced by the relaxation time between current pulses [40], also called the recovery effect.

Discharging batteries have a profile displayed in Figure 4-32, with an obvious voltage drop/decline. The discharge curve plateaus into what is known as the nominal cell voltage. The main reason for the discrepancy between open-circuit voltage and the nominal voltage is the internal equivalent resistance dissipating a fraction of the cell power.
As the cell reaches a depleted state, the voltage quickly falls down to zero; however, realistic end-of-life voltages are usually 70-80\% of the plateau voltage, expressed as the Minimal Voltage. Depleting a battery beyond this point may leave rechargeable batteries damaged and in extreme cases, batteries undergo voltage reversal that may damage a system.

To summarize the discussion on batteries,

Table 4-15 shows commercially available batteries:

<table>
<thead>
<tr>
<th>Battery Chemistry</th>
<th>Self-discharge capacity/month</th>
<th>Operating temperature °C</th>
<th>Power density W·h/kg</th>
<th>Relative cost (1-6)</th>
<th>Nominal voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Secondary</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ni-MH</td>
<td>30</td>
<td>-20</td>
<td>30-80</td>
<td>3</td>
<td>1.2</td>
</tr>
<tr>
<td>Ni-Cd</td>
<td>20</td>
<td>-40</td>
<td>40-60</td>
<td>4</td>
<td>1.2</td>
</tr>
<tr>
<td>Lead Acid</td>
<td>30-20</td>
<td>-40</td>
<td>30-40</td>
<td>2</td>
<td>2.0</td>
</tr>
<tr>
<td>Li-ion</td>
<td>8</td>
<td>-20</td>
<td>100-265</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td>Li-Pol</td>
<td>5</td>
<td>-20</td>
<td>130-200</td>
<td>6</td>
<td>2.5</td>
</tr>
<tr>
<td>Primary</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Alkaline</td>
<td>0.17</td>
<td>-20</td>
<td>85-190</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>Carbon-Zinc</td>
<td>0.32</td>
<td>-20</td>
<td>36</td>
<td>1</td>
<td>1.5</td>
</tr>
<tr>
<td>Silver Oxide</td>
<td>0.7</td>
<td>-20</td>
<td>130</td>
<td>1</td>
<td>1.6</td>
</tr>
<tr>
<td>Lithium Manganese Dioxide</td>
<td>0.1</td>
<td>-20</td>
<td>100-150</td>
<td>6</td>
<td>3.0</td>
</tr>
<tr>
<td>Lithium Sulphur Dioxide</td>
<td>0.1</td>
<td>-55</td>
<td>250</td>
<td>5</td>
<td>3.0</td>
</tr>
</tbody>
</table>
Of all the batteries available, lithium / thionyl chloride (Li /SOCl2) shows the highest energy density. These lithium primary cells have been specifically designed for low temperatures, only freezing below –105 °C [47], making them the best candidate for low-temperature applications.

4.5.3 Solar power

Given the right location, solar power is a readily available power source. Solar cells combined with a battery storage system can provide constant power to a system. The average photovoltaic (PV) cell has lifetime of 30 years, with maintenance only required for the battery system.

The fundamental component of a solar panel is the PV cell. As photons hit the surface of the cell, electrons are displaced, causing a voltage drop across the interface; this allows a current to flow towards the connected terminal.

Combining these cells into series chains allows panels with high voltages, and by configuring theses chains into parallel groups the panel current rating is increased. The electric properties of a solar panel can be characterized by certain parameters:

- Open circuit voltage \( V_{oc} \);
- Short circuit current \( I_{sc} \).

A solar panel behaves as a voltage-limited current source, dependent on the amount of incident solar radiation. Therefore, decreasing radiation will proportionally decrease the current \( I_{sc} \), whilst the voltage \( V_{OC} \) remains relatively constant.

This current source behaviour makes the output voltage highly dependent on the load impedance, as a result making it difficult to power a system directly from a panel. Hence, an energy storage unit is needed to store the harvested energy and provide a stable voltage to the system [48].

On average, one square meter of full sunlight delivers about 1 kW of energy [46]. Therefore with 12 hours of direct sunlight available, a square meter surface should deliver 12 kWh per day. However, with practical PV systems this is not the case. Two factors that determine the PV system power output are shown to be:

Solar angle

Solar energy is dependent on the angle of the sun’s rays hitting the incident surface. Assuming a flat terrestrial surface the available daily energy, as a function of day of year and physical latitude, is shown in Figure 4-33.
From this figure, it is clear that solar energy at the Polar regions is available for only half the year. Consequently, solar power for an autonomous observatory is only possible within the summer months.

**PV efficiency**

The second power limiting factor that must account for PV systems is the PV cell efficiency. Panel technology is currently available in three types:

<table>
<thead>
<tr>
<th>Type</th>
<th>Efficiency (%)</th>
<th>Cost</th>
<th>Technology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mono crystalline</td>
<td>19-25</td>
<td>Expensive</td>
<td>Single Silicon crystals</td>
</tr>
<tr>
<td>Poly crystalline</td>
<td>18</td>
<td>Cheaper</td>
<td>Multiple crystals</td>
</tr>
<tr>
<td>Thin-film</td>
<td>8</td>
<td>Cheapest</td>
<td>Photo reactive material</td>
</tr>
</tbody>
</table>

It is shown that panel efficiency ranges between 8 to 25% efficiency, thus the maximum amount of energy that can be obtained for a solar panel would be $125 \text{ Wh} \cdot \text{m}^{-2} \cdot \text{day}^{-1}$.

**Temperature effects**

PV panels, which are basically semiconductor interfaces, show the same low temperature effect as that of diodes and transistors. Thus, PV cells show increased junction voltage at lower temperatures. It is commonly better to keep a PV system cool rather than hot, consequently increasing efficiency. This effect is expressed by the power temperature coefficient $M_{MPP}$, indicating the percentage differential change from the nominal (25 °C) open-circuit voltage.
With a $M_{\text{MPP}}$ value of $-0.5 \% / ^\circ \text{C}$ and an ambient temperature of $-75 ^\circ \text{C}$, the cell voltage can potentially be double of that of a panel at $25 ^\circ \text{C}$. Thus, the implementation of the power converter must be robust enough to take this increased voltage into account.

Although Antarctic conditions would only provide solar power for less than half a year, implementation of a solar power ad-hoc power source will decrease the system’s annual power requirements and therefore cost.

### 4.5.4 Wind power

An alternative source of energy is that of wind power. This harvesting technology relies on the kinetic flow of air, therefore wind is converted to electricity. The seasonal and location dependence of wind makes the availability inconsistent. Therefore it is only suitable as an augmented power source.

Available power, $P_{\text{avail}}$ of a vertical wind turbine can be shown to be:

$$P_{\text{avail}} = \frac{1}{2} \rho A v^3 C_P,$$

where $A =$ blade sweep area,
$v =$ wind velocity,
$\rho =$ air density, and
$C_P =$ power coefficient.

Albert Betz concluded that wind turbines cannot convert more than 59.3 % of wind kinetic energy. Thus the theoretical efficiency of any vertical blade design is limited to between 35 to 45 %. By using an air density of 1.23 kg $\cdot$ m$^{-3}$ and power coefficient of 0.3 and 0.1 m blade length, possible power outputs can be shown to be:

<table>
<thead>
<tr>
<th>Wind speed (kn)</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1.547 mW</td>
</tr>
<tr>
<td>5</td>
<td>197 mW</td>
</tr>
<tr>
<td>10</td>
<td>1.57 W</td>
</tr>
<tr>
<td>15</td>
<td>5.31 W</td>
</tr>
<tr>
<td>20</td>
<td>12.59 W</td>
</tr>
</tbody>
</table>

At the proposed Antarctic coast locations, winds are relatively high, with the moderate winds on the plateau. Katabatic winds tend to be more active during the winter months [50], therefore making it possible to augment power when solar power is unavailable. Table 4-17 shows that a one watt system can be possibly be augmented, given the availability of a moderate 5-10 knot wind.
However, the extreme Antarctic conditions subject a system to a variety of mechanical stresses, consequently affecting the reliability of such a system.

Environmental effects / Cold climate issues:

- **Extreme temperatures**, as discussed in Section 4.3.2. Materials exhibit different properties as different temperatures. Therefore a turbine would have to be designed for both cold start and running conditions.

- **Icing**: Occasional snow storms, condensation and operation in warm conditions may lead to blades icing up. As an automated system, lack of maintenance may prove to be problematic.

- **Strong winds**: Although annual plateau wind speeds may be moderate, there are cases where storms occur with extremely high peak wind speeds. This may exceed the turbine operating condition. Therefore additional over-speed protection is needed.

- **Static electricity**: The extreme low humidity of Antarctic air and the lack of proper grounding leads to static build-up on any synthetic surface. This consequently leads to electrostatic discharges, damaging electronic systems.

- **Snow and moisture ingress**: Snow and vapour particles are extremely small, therefore very difficult to protect against, especially in the case of the shaft and bearings. Any moisture inside the system will ice up and damage the system.

- **Logistics**: The wind turbine requires a vertical standing structure, thus requiring the transportation and setup of a pole and stays.

In an autonomous system, the environmental circumstances greatly affect reliability and as a result this system cannot be used as the primary source of power. If used, it would rather be prudent to use a turbine to augment the current power source. This will increases the overall system power availability and in the event of turbine failure, not lead to overall system failure.

### 4.6 Data storage

Fundamental to an automated data capturing system is its ability to store all the collected data, therefore it must have sufficient storage available. A review of the currently available data storage systems will be addressed in this section.

#### 4.6.1 Hard drive

The original CNM, as discussed in section 4, used a standard PC hard drive. A hard drive is excluded as a design option due to the following characteristics:

- These drives use excessive amounts of power;
- Use higher level interfaces, requiring complex circuit integration;
- Are mechanical in nature, therefore susceptible to low-temperature failures;
- Hard drives are supplied in large sizes and thus costly for small data sets.
4.6.2 Flash memory

Flash memory is the most common data storage used in automated data capturing. Its high reliability, low power consumption and relatively small size make it ideal for portable applications.

Flash memory is “Non Volatile Solid State Storage” using floating gate transistors. It is within this floating gate that a charge is placed, allowing the storage of binary 1’s or 0’s. There are two types of flash memory, named after the NAND and NOR logic gates, which the floating gate resembles.

A significant limitation of flash memory is that it has a finite number of program and erase (P/E) cycles; thereafter a memory cell becomes unreliable. Additionally to NAND and NOR topologies, flash also comes in three technologies, namely:

- **Single-level cell** (SLC) memory uses a single floating gate to store one bit of data. As a result the P/E per cell cycle wear is one to one, making this type of memory the most reliable for industrial applications. The standard endurance for SLC flash storage is ~100 000 P/E cycles;

- **Multi-level cell** (MLC) flash memory has four possible states per cell, so it can store two bits of information per cell. This reduced level separation results in the possibility of more errors, therefore requires more power per write to validate data. This also increases the memory density, but in so doing reduces the durability of the gate. The standard endurance for MLC memory is between 3 000-5 000 P/E cycles;

- **Triple-level cell** (TLC) memory increases the memory density further by using additional states to eight total states increasing data per cell. Because of this higher density, performance and endurance is lowered. The standard endurance for TLC is ~2 000 P/E cycles.

Both memory types are produced in serial and parallel interfaces. By using a serial interface the number of external pins can be reduced. Smaller and lower pin-count packages occupy less PCB area. Lower pin-count devices also simplify layout routing.

However, the use of integrated flash memory ICs requires the interface of a controller, to manage the memory addressing and the state of P/E wear cycles. Wear-levelling is the process of spreading P/E cycles, hence data-blocks, evenly across the entire memory, extending the life of the memory module [55].

It was deemed unpractical to use flash memory ICs. The wear of memory cells would eventually leave the memory unusable, requiring the replacement of the memory IC.

4.6.3 USB mass storage

On the other hand, Universal serial bus (USB) mass storage drives are removable flash storage devices, equipped with a USB interface. The USB communications standard has become one
of the most common interface technologies within the computer industry. As a result USB data storage devices have become one of the most accessible storage mediums on the market.

A USB flash drive, otherwise referred to as a ‘thumb drive”, is a data storage device, typically using existing NAND flash technology integrated with an MCU controller. Based on NAND flash memory, USB flash drives are subject to the same memory wear issues as those of standard flash storage. However, in contrast to the IC technology, USB flash drives include an embedded controller that can manage wear levelling.

The P/E endurance and current consumption of USB are shown to be:

<table>
<thead>
<tr>
<th>USB Flash</th>
<th>Memory type</th>
<th>Temperature °C</th>
<th>Supply voltage</th>
<th>Average power (mW)</th>
<th>P/E cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>TLC</td>
<td>-10 to 85</td>
<td>5.0 V</td>
<td>Read 310</td>
<td>~3 000</td>
</tr>
<tr>
<td>Industrial</td>
<td>MLC</td>
<td>-40 to 85</td>
<td>Idle 3</td>
<td>Write 350</td>
<td>~5 000</td>
</tr>
</tbody>
</table>

The MNM, as discussed in Section 4, used USB media as a back-up storage device. Almost all mainstream operating-systems support USB thumb drives, making it an ideal technology for use in data-logging applications.

Currently the USB 3.0 standard allows for the transfer of data rates up to 625 Mb/s and the interface requires a fixed operating frequency, therefore it does not allow the slowing down of the interface clocking frequency. This increases the consumption and complexity of the interface. However, it was also found that USB flash drive power consumption varied significantly from one product to another, even from the same manufacturer. Power consumption was also found to be proportional to the size of memory in use. Selecting a smaller memory module will consequently reduce power consumption.

The use of USB flash drives will also be excluded for the following reasons:

- USBs require a fixed 5 V operating voltage to function;
- The protocol runs at a high operating frequency;
- The USB protocol layer requires a higher overhead performance form an MCU.

### 4.6.4 SD/MMC

Another form of removable data storage is that of Multimedia cards (MMC). SanDisk and Siemens AG developed the first MMC standard in 1997. Similar to USB flash, the MMC is NAND flash, integrated with a microcontroller. The primary difference is that of the form factor which is the size of a postage stamp and the interface that is a 7-pin serial interface.

The interface allows full control of low-voltage flash memory, allowing erasing, reading, writing, error control monitoring and wear level function to be executed.
Using flash-memory cards rather than raw flash chips has two advantages. The controller in the card greatly simplifies accessing the memory. Cards also are easily removable and replaceable, so one can store data in multiple cards and replace cards that fail or wear out. An autonomous logger would ideally require a form of memory that can be removed and replaced. Unlike the USB flash MMCs are more tolerant of various operating voltages and do not require a fixed frequency to interface. Therefore it is more dynamic for use with low-power applications. Multimedia cards use minimal power.

Table 4-19 SD/MMC card specification

<table>
<thead>
<tr>
<th>Type</th>
<th>Memory type</th>
<th>Temperature °C</th>
<th>Supply voltage</th>
<th>Average power (mW)</th>
<th>P/E cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial</td>
<td>TLC</td>
<td>-25 to 85</td>
<td>2.7-3.6 V</td>
<td>Read 144</td>
<td>~3 000</td>
</tr>
<tr>
<td></td>
<td>MLC</td>
<td></td>
<td></td>
<td>Write 158</td>
<td>~5 000</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Idle 1</td>
<td>~100 000</td>
</tr>
</tbody>
</table>

Power consumption compiled from various product datasheets shown in the Appendix

As a later development Secure Digital (SD) cards were introduced by Toshiba, Matsushita Electric (Panasonic), and SanDisk in 1999. The SD card expanded the 1-bit interface of an MMC to a parallel 4-bit proprietary interface, but still remained backward compatible to the original MMC interface standard.

Table 4-20 Range of SD card sizes

<table>
<thead>
<tr>
<th>Types</th>
<th>Size (GB)</th>
<th>SD BUS speed (Mb/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard-capacity</td>
<td>SDSC</td>
<td>&lt; 4</td>
</tr>
<tr>
<td>High-capacity</td>
<td>SDHC</td>
<td>&lt; 32</td>
</tr>
<tr>
<td>Extended-capacity</td>
<td>SDXC</td>
<td>&lt; 2 000</td>
</tr>
</tbody>
</table>

As with USB, memory size was found to increase the power consumption of the memory in use. Thus, SDHC card average power consumption was found to be higher than that of a smaller capacity SD card.
The benefit of using MMC/SD is that most MCUs include hardware support for SPI interface. The SD cards typically draw no more than 100 mA of current while active, and can operate at a lower 2.7 V, thus drawing significantly less power than both CF or USB devices. If power consumption is important, SD again is a good choice.

The primary design considerations of interest are:

- **Low-temperature**: all three options IC Flash, USB and MMC/SD come in industrial rated version;

- **Low-power**: it is clear that MMC/SD cards show the best low-power characteristics, both on a performance level and complexity level. A USB operating at 5 V and requiring the implementation of the complex USB interface is both time and energy consuming;

- **Complexity**: lastly the IC Flash is a good option, with the exception that all the built-in functionality imbedded within MMC/SD has to be developed by the designer.

Thus it is clear from this analysis that the MMC/SD is the best option for a low-temperature, low-power and least complex implementation for data storage.

### 4.7 Autonomous systems design

An autonomous systems design implies an independent, fault-tolerant smart system, with no need for supervision that can operate appropriately in an uncertain environment. This autonomous behaviour increases the probability of systems success.

Because autonomous operation encompasses a broad spectrum of topics, this research will define autonomous operation as:

- Self-governing, stand-alone device defined as systems that can function independently of either external hardware or other services. It is a self-contained device capable of
performing a specific set of functions. The most common function is the ability to log sensor data over time; data loggers are implicitly stand-alone devices. Outside the device’s primary functions the following specifications must be assessed:

- Reliable operation:
  - Diagnostic;
  - Fault tolerant;
  - Fault recovery.

It is not possible to develop a system with zero failure rates. Reliability is imperative because a stand-alone device has no external service to maintain the system. A system that fails within its operational lifetime may not necessarily be repaired, especially if it is deployed in an inaccessible location. A system tends also to become more vulnerable to failure the more functions it has to perform.

Systematic Failures

- Design or manufacturing defects;
- Rate of systematic failures can be reduced through continual and rigorous process improvement;
- Random failures: defects inherent in the system.

4.7.1 Simplicity

In a complex MCU system, scheduling is needed when multiple functional units need to access the MCU. With increased complexity, defects may be introduced by mistakes. Keeping the MCU software as simple as possible, limits the introduction of task-related faults.

4.7.2 Recovery

Provision has to be made within the software to recover from coding-related fault conditions. Service routines operate relatively independently; it is very possible for some to be alive while others are locked, dead, or executing nonsensical code. Some examples of code failures are:

- Program-flow/operating system failure;
- Infinite loop;
- Deadlock involving priority task clashes (low priority task being neglected because of higher priority tasks).

4.7.3 Power management

Voltage supervision – Brown-Out detection

To function, a system requires energy and an automatic device should be able to manage its energy source. In the case of most portable applications that source is usually a battery system.
Electronic systems seldom operate at the desired cell voltage, and even if it is the case, efficiency varies. Complex circuits also tend to have multiple voltage requirements, therefore requiring a management system to address these needs.

4.7.4 Memory

The previous specification determines the capacity requirement of a device. For each sample a data-specific memory is required. A higher sample rate will have a reduced operational time.

The primary goal of a data logger is inherently to collect and preserve data and samples taken from its various sensors. Furthermore as an autonomous observatory, data should be preserved in a reliable manner. Therefore the data quality is of importance. The two types of errors that may occur in a system are hardware and software related errors.

Data transmission can contain the following errors:

- Single-bit;
- Burst errors of length $n$.

The way in which data is stored and protected against failure and errors occurring within the data wiring and storage process influences the quality of the data. For this reason redundancy and error checking are necessary. This can be achieved with firmware algorithms and technology.

4.8 Antarctic weather

As mentioned in Section 4, the new Low Power/Low Temperature Neutron Monitor (LPT-NM) will be required to operate in Antarctica, consequently low temperatures must be taken into account.

The coastal winter monthly mean is between $-10 \, ^\circ\text{C}$ and $-30 \, ^\circ\text{C}$, while the plateau averages between $-40 \, ^\circ\text{C}$ to $-60 \, ^\circ\text{C}$. Conditions on the high interior plateau are much colder as a result of its higher elevation, because of higher latitude, and greater distance from the ocean. Vostok station holds the record at $-89.2 \, ^\circ\text{C}$, the lowest surface temperature ever recorded [51].

Other than the cold, additional hazardous effects are also prevalent in Antarctica. Snow particles and moisture infiltrate equipment through gaps and cracks. Combined with internal thermal cycling, moisture may freeze, melt and condense (freeze-thaw), damaging any exposed components inside.

4.8.1 Ingress protection

Therefore, an enclosure with Ingress Protection (IP) is needed. The IP rating is an international standard for sealed devices, with two numbers indicating the level of protection. The first number reflects the protection against solid objects while the second number shows protection against liquids.

The first number:
Protection against solid objects larger than:

1. 50 mm, e.g. hands;
2. 12 mm, e.g. fingers;
3. 2.5 mm, e.g. tools;
4. 1.0 mm, e.g. wires;

Dust protection:

5. Limited ingress of dust, not interfering with equipment;
6. Totally protected against dust.

**Second number:**

Protection from water:

1. Vertically falling drops or condensation;
2. Sprayed at a 15 ° angle, e.g. light rain in wind;
3. Sprayed at a 60 ° angle, e.g. heavy rainstorm;
4. Sprayed from all directions;
5. Low pressure nozzle spray, e.g. residential hose;
6. High pressure, powerful jets of water;
7. Temporary protected from 15 cm to 1 m immersion in water;
8. Protected against complete continuous submersion in water.

*It was shown that the ingress expected would be snow-particulates, condensing moistures and in certain cases water from thawed ice, therefore a practical rating for the autonomous NM would be IP67.*

### 4.8.2 Seals

Cable and conduit gasket seals make up the fundamental blocks of a rated enclosure. Although enclosures are manufactured to a specific IP rating, they are only as good as the seals used to provide access to the external environment. Additionally, the IP rating does not address the low temperature specifications needed. Therefore the selection of gasket seal material must be considered. In the case of this study, the functional life of gasket seals will depend on exposure to large temperature range, mechanical wear and possibly UV radiation.
Table 4-21 Type of seal gaskets

<table>
<thead>
<tr>
<th>Materials</th>
<th>Temperature range (°C)</th>
<th>UV resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Neoprene Rubber</td>
<td>-20 to 90</td>
<td>✓</td>
</tr>
<tr>
<td>Natural Rubber</td>
<td>-30 to 80</td>
<td>×</td>
</tr>
<tr>
<td>Silicone Rubber</td>
<td>-50 to 250</td>
<td>✓</td>
</tr>
<tr>
<td>Closed Cell Silicone Sponge Rubber</td>
<td>-85 to 400</td>
<td>✓</td>
</tr>
</tbody>
</table>

Table 4-21 therefore shows that for weather proof sealing, silicone sponge is the best material choice for an extreme temperature environment.

Seal gaskets are also manufactured and provided in different forms, two of which are:

- Stripping, rolls of material cut in specific widths that can be cut to length by the designer. This is a low-cost option, however, seems to make the system susceptible to leakage.

- Die-cut is a seamless cut gasket, eliminating corner seams. This insures a more secure seal, preventing any ingress failure due to seams. Using and implementing this type is more complex, requiring design considerations, which leads to increased cost.

4.9 Conclusion

In this chapter, a study was done on thermal dynamics, including thermal constraints and insulation. The behaviour of electronics at low temperatures was studied, with specific attention to component ratings, physical effects at low temperatures, and design methods for low temperatures.

Low power design was studied for hardware and software, and micro-power measurements were studied to understand the principles of measurement accuracy.

Energy storage had to be studied to address the requirement for standalone operation. Different power supply options were considered, and battery technologies were evaluated for this application.

Since the neutron monitor will have to store data, different storage options were considered, given low temperature and power considerations.

Attention was given to autonomous system design, as the system is essentially autonomous in nature. Specific attention was given to simplicity, recovery, power management, and data storage.

Finally, Antarctic weather conditions were analysed and specific attention was given to ingress protection.
In summary, the research challenges and literature focus areas as discussed in this chapter are shown in Table 4-22. The table shows how each literature topic lines up with different research challenges. This matrix will be used to show how a solution was obtained by using information from the literature study later on in this document.

Table 4-22 Literature study focus areas applicable to the research challenges

<table>
<thead>
<tr>
<th>Literature focus areas</th>
<th>Research challenges</th>
<th>Extreme environmental conditions</th>
<th>Operation in remote locations</th>
<th>Logistical constraints</th>
<th>Limited budget</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. Thermal dynamics</td>
<td>↑↓↓</td>
<td>↓</td>
<td>↑</td>
<td>↑</td>
<td></td>
</tr>
<tr>
<td>2. Low-temperature electronics</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Behaviour</td>
<td>↑↓</td>
<td>↓</td>
<td>↑</td>
<td>↓</td>
<td></td>
</tr>
<tr>
<td>3. Low-power circuit design</td>
<td>↑</td>
<td>↓</td>
<td>↑↓</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4. Electronic energy/power sources</td>
<td>↑</td>
<td>↓</td>
<td>↑</td>
<td>↑↓</td>
<td></td>
</tr>
<tr>
<td>5. Data storage systems</td>
<td>↑</td>
<td>↓</td>
<td>↓</td>
<td>↓</td>
<td></td>
</tr>
<tr>
<td>6. Environmental protection</td>
<td>↑↓</td>
<td>↓</td>
<td>↓</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Literature focus areas</th>
<th>Research solutions</th>
<th>Robust electronics</th>
<th>Mechanical implementation</th>
<th>Autonomous operation</th>
<th>Design for transportability</th>
<th>Low cost design</th>
</tr>
</thead>
</table>

Legend: ↑ - Literature focus area validates the research challenge
↓ - Literature focus area contributes to the research solution
5 Synthesis

5.1 Introduction

This chapter focusses on the detailed design of a conceptual system, primarily that of the:

- Neutron monitor data acquisition unit:
  - Electronics;
  - Software/Firmware;

- Mechanical enclosure.

According to the DSR methodology and the research objectives defined in Section 3.5, the outcomes for this research can be grouped into four distinct categories, namely constructs, methods, models, and instantiations.

The DSR model maturity (as defined in Section 2.5.1) is that of an improved variant of the existing MNM system and the DSR construct is a design document for a LPT-NM.

![Figure 5-1 Flow of DSR deliverables](image)

Figure 5-1 shows the flow for all methods as they lead to models. From these models an artefact and meta-artefacts were created. The artefact that was developed is the NM-DAS, with its accompanying mechanical design. The mechanical design is presented as a theoretical concept.
design (therefore, a DSR model) as the physical implementation falls outside the scope of this work.

### 5.2 Feasibility study

Before any design could be considered, the fundamental question of feasibility of solutions had to be addressed, specifically the existing MNM-DAS architecture which was shown in Figure 3-6, and the system shortfalls described in Section 3.2.2. The two main areas of investigation were the system’s thermal and power budget requirements.

#### 5.2.1 MNM power requirement

As indicated in Section 3.2.2, the existing MNM consumes up to 2.5 W of electrical power. Using batteries to power the system, rather than mains, Table 5-1 shows the amount of batteries required to power an existing MNM system. Section 4.4.2 showed that the lithium/thionyl chloride (Li/SOCl\textsubscript{2}) is the ideal battery solution for a low-temperature environment. Remaining options would be larger and more expensive. Therefore, the evaluation below was limited to a Li/SOCl\textsubscript{2} battery solution.

<table>
<thead>
<tr>
<th>Period</th>
<th>Hours</th>
<th>Power (Wh)</th>
<th>Number of batteries</th>
<th>Mass (kg)</th>
<th>Volume (litre)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Day</td>
<td>24</td>
<td>60</td>
<td>0.5</td>
<td>0.08</td>
<td>0.04</td>
</tr>
<tr>
<td>1 Month</td>
<td>~720</td>
<td>1 800</td>
<td>15</td>
<td>2.5</td>
<td>0.78</td>
</tr>
<tr>
<td>1 Year</td>
<td>8 760</td>
<td>21 900</td>
<td>184</td>
<td>30</td>
<td>15.4</td>
</tr>
</tbody>
</table>

It is clear that a 2.5 W MNM system would require an unrealistic number of batteries, making it costly, large and therefore unsuitable for use in an autonomous instrument. For this reason, the system’s power consumption had to be lowered to a more achievable value.

#### 5.2.2 MNM heating requirement

A simplistic thermal conduction model was developed to evaluate the existing MNM system. The model shown in Figure 5-2 describes the conduction of heat generated by the system to its external environment, given a certain amount of insulation, thus, describing the low-temperature operational limits of the system.

The model makes use of an enclosure, reduced to thin layers of insulation material. With each additional layer, the thermal conducting surface of the enclosure is increased, effectively reducing the thermal resistance of the insulating barrier.
Assuming a cubic volume, the surface area for each layer within the enclosure was calculated using:

\[ A_n = \text{area of the specific conducting layer } n, \]

where \( A_n \) = area of the specific conducting layer \( n \),

\[
A_n = 2 \times ( [w_0 + 2nL][l_0 + 2nL] + [w_0 + 2nL][h_0 + 2nL] + [l_0 + 2nL][h_0 + 2nL] ) \tag{5-1}
\]

\( L \) = layer thickness,

\( w_0 \) = enclosure internal width,

\( l_0 \) = enclosure internal length, and

\( h_0 \) = enclosure internal height.

The following discussion assesses this expression for the heat-transfer process of conduction, convection and radiation.

**Conduction:** With the area known, the conduction Equation 4.3 can be used to calculate the differential temperature for each layer.

Section 3.2 showed the MNM initial surface to be 0.088 m\(^2\) and the heat generated to be 2.5 W. Thus by using VIP insulation, described in Section 4.1.1, with a thermal conductivity of 0.004, the temperature differential was calculated to be 60 °C across 10 mm of insulation.

**Convection:** Since the enclosure lacks airflow to the external environment, convection is assumed to be limited to the transfer of energy from the PCB to the enclosure internal air volume. Because this creates a uniform temperature within the enclosure, the effects of convection can be ignored.

**Radiation:** Using Stefan’s law in Section 4.2.1, the effect of radiation for a 0.088 m\(^2\) surface, with a temperature 60 °C above ambient was approximated to between 19 – 309 μW assuming a emissivity’s between of 0.06 – 0.96. Because this was significantly smaller than conductive heat, the effect was also ignored.
Thus the system was modelled based on the process of conduction. It was concluded that the 2.5 W MNM would generate sufficient thermal energy to maintain a temperature gradient of 60 ºC above the ambient, using a single 10 mm VIP panel.

By increasing internal power of the internal electronics and thus the heat generated by circuitry, it was possible to obtain an estimate of the temperature differential that could be obtained for 10 mm and 200 mm insulation thicknesses. The following table shows the energy required to maintain a temperature differential of 40 ºC between internal circuitry and the external environment.

<table>
<thead>
<tr>
<th>Power mW</th>
<th>VIP thickness 10 mm</th>
<th>VIP thickness 200 mm</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>1.18</td>
<td>6</td>
</tr>
<tr>
<td>100</td>
<td>2.3</td>
<td>12</td>
</tr>
<tr>
<td>150</td>
<td>3.56</td>
<td>18</td>
</tr>
<tr>
<td>200</td>
<td>4.7</td>
<td>24</td>
</tr>
<tr>
<td>250</td>
<td>5.94</td>
<td>32</td>
</tr>
<tr>
<td>300</td>
<td>7.12</td>
<td>38</td>
</tr>
<tr>
<td>350</td>
<td>8.3</td>
<td>44</td>
</tr>
<tr>
<td>MNM →</td>
<td>2500</td>
<td>60</td>
</tr>
</tbody>
</table>

Common industrial electronic components are typically rated to operate at temperatures down to -40 ºC while the external environment has temperatures down to -80 ºC. Therefore, to maintain an enclosure internal temperature above -40 ºC, from the table it can be seen that a minimum of 350 mW and 200 mm of VIP insulation panelling would be required.

5.3 Synthesis and evaluation

This section considers the three main objectives by focusing on the methods that were used to achieve these objectives, followed by the models that were generated and the physical constructs that were built.

In all design phases, low-power and low-temperature operation were taken into account. The section concludes by showing empirical results obtained from testing and evaluating the physical constructs.

5.3.1 Electronic design

The first step in the design process was to address the electronic data capturing sub-system. Although the focus is on the electronic design, the electronic design was executed concurrently with the software design. As shown in Figure 5-3, the data capturing sub-system was divided into software and hardware categories.
Hardware and software combine to provide functionality required for interfacing I/O, processing and data storage, as is common to embedded systems. The figure below provides a breakdown of hardware and software modules that make up the data capturing sub-system by showing these modules in a logical design flow sequence (top to bottom).

### Component selection and design method

A modular design approach was used to also allow synthesis and evaluation of individual sub-systems and modules. Because of this approach, each sub-system could be designed, modelled, and evaluated as a separate entity, reducing the overall system’s development time and risk, and reducing future maintenance and repair efforts and costs.
Each sub-system went through the same process of selection and synthesis as shown in Figure 5-4:

**Figure 5-4 Design flow of individual modules**

Based on specific sub-system specifications, the first step involved planning of hardware architecture. This high-level conceptual design was based on all external requirements including at least power, temperature and interface constraints.

By first defining functional units and interfaces, physical components were selected to satisfy the system and sub-system requirements. Component selection was critical to ensure both low-power and low temperature design requirements were met. All components had to:

1. Fulfil a specific function, to satisfy their functional requirements;
2. Operate at low-temperatures -40 °C;
3. Be low-power components.

**Design (models)**

This section describes the modular design of hardware layers as shown in Figure 5-4.

**Controller**

The MCU requirements were based on the architecture shown in Figure 3.5. Because of the existing MNM shortfalls, the architecture had to be changed. Table 5-3 shows the changes that were made to the existing MNM design.
Table 5-3. Systems architecture changes

<table>
<thead>
<tr>
<th>MNM DAS Old</th>
<th>LPT-NM New</th>
<th>Motivation</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD/LEDs</td>
<td>Removed</td>
<td>Redundant feature</td>
</tr>
<tr>
<td>Ethernet module</td>
<td>Removed</td>
<td>Redundant feature</td>
</tr>
<tr>
<td>User IO</td>
<td>Buttons were removed</td>
<td>A PC USB interface was added</td>
</tr>
<tr>
<td>Linear voltage regulators</td>
<td>High efficiency switch mode</td>
<td>Lower power consumption</td>
</tr>
<tr>
<td>High voltage supply</td>
<td>Alternate component programmable/ internal measurement</td>
<td>Low temperature supply needed</td>
</tr>
<tr>
<td>USB flash drive</td>
<td>MMC/ SD</td>
<td>Lower power consumption</td>
</tr>
<tr>
<td>Resistive temperature Sensor</td>
<td>Digital temperature sensor</td>
<td>Reduced complicity</td>
</tr>
<tr>
<td>High performance PIC32MX MCU</td>
<td>Low power alternative MCU</td>
<td>Lower power consumption</td>
</tr>
</tbody>
</table>

Based on these modifications, Figure 3.5 was adapted to a new sub-system architecture as shown in Figure 5-5.

Four primary specifications were used to evaluate MCUs as candidates for addressing the requirements of the new system architecture.

- The MCU peripherals USART, I2C, SPI and ADC were assigned a value out of four for each candidate MCU;
• The NWU cosmic-ray project lab had been making use of development tools for the construction of the MNM. Available development tools were assigned a 0 or 1 value;

• It was assumed that the sub-system would be using power scheduling as described in Section 4.3.2 to reduce power consumption. The sub-system would thus be running only for short periods during sampling while sleeping between data capture sessions. A 20 % running versus 80 % sleep mode was used as a reference and the normalized power consumption for each candidate was used as a measure;

• Finally, the candidate’s minimum operating voltage was considered.

<table>
<thead>
<tr>
<th>Table 5-4 Decision matrix selection of MCU</th>
<th>Peripheral functions available</th>
<th>Development tools available</th>
<th>20 / 80 Dynamic versus static duty cycle</th>
<th>Voltage below 3.3 V (V)</th>
<th>MCDM score</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td></td>
<td></td>
<td>Normalized power</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PIC32MX</td>
<td>4</td>
<td>1</td>
<td>0.08</td>
<td>1</td>
<td>6.08</td>
</tr>
<tr>
<td>MSP430</td>
<td>4</td>
<td>0</td>
<td>1.05</td>
<td>1.5</td>
<td>6.55</td>
</tr>
<tr>
<td>STM32 L0</td>
<td>4</td>
<td>0</td>
<td>0.36</td>
<td>1.5</td>
<td>5.86</td>
</tr>
<tr>
<td>XMEGA</td>
<td>4</td>
<td>0</td>
<td>0.31</td>
<td>1.7</td>
<td>6.01</td>
</tr>
<tr>
<td>PIC16F1509</td>
<td>1</td>
<td>1</td>
<td>2.69</td>
<td>1.5</td>
<td>6.19</td>
</tr>
<tr>
<td>PIC24FJ64GB004</td>
<td>2</td>
<td>1</td>
<td>0.44</td>
<td>1.3</td>
<td>4.74</td>
</tr>
<tr>
<td>PIC24FJ128GA310</td>
<td>4</td>
<td>1</td>
<td>0.72</td>
<td>1.3</td>
<td>7.02</td>
</tr>
<tr>
<td>C8051F96x</td>
<td>4</td>
<td>0</td>
<td>0.80</td>
<td>1.5</td>
<td>6.3</td>
</tr>
</tbody>
</table>

Based on a score of 7.02, the PIC24FJ128GA310 MCU was found best suited for this sub-system.

To allow low power operation, a dual clock system was selected, allowing dynamic switching between two clock sources - therefore two separate internal crystal oscillators were required.

Crystal oscillators can be affected by temperature. Consequently, crystal selection was simply based on well-documented crystal specifications, requiring temperature stability down to -40 °C.

The primary crystal was selected at a resonance frequency of 24.576 MHz to support fast and precise UART communication, whilst the secondary low-power crystal was selected at 32.768 kHz specifically for the purpose of the real-time clock.

Because manufacturer documentation refers to pre-defined operating conditions, the power budget estimation was done for 1 MIPS and 12 MIPS with the operating voltage set at 3.3 V.
Table 5-5. Power budget for MCU

<table>
<thead>
<tr>
<th>MCU functions</th>
<th>Active current (µA)</th>
<th>Active time (%)</th>
<th>Subtotal currents (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mode</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RUN</td>
<td>150 / 1800</td>
<td>0.2</td>
<td>30 / 360</td>
</tr>
<tr>
<td>IDLE</td>
<td>86 / 1036</td>
<td>0.1</td>
<td>8.6 / 103</td>
</tr>
<tr>
<td>SLEEP</td>
<td>3.8</td>
<td>0.7</td>
<td>2.66</td>
</tr>
</tbody>
</table>

Peripherals

<table>
<thead>
<tr>
<th>Peripherals</th>
<th>Number of peripherals × Duty cycle</th>
<th>Current</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>WDT</td>
<td>0.8 1 × 1</td>
<td>0.8</td>
<td>0.8</td>
</tr>
<tr>
<td>RTCC</td>
<td>0.4 1 × 1</td>
<td>0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>Timer Counter</td>
<td>1 1 × 1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Comparator</td>
<td>28 1 × 1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>VREF Pin</td>
<td>1 1 × 1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>I2C</td>
<td>1000 1 × 0.2</td>
<td>200</td>
<td>140</td>
</tr>
<tr>
<td>SPI</td>
<td>700 1 × 0.2</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>USART</td>
<td>200 2 × 0.2</td>
<td>80</td>
<td></td>
</tr>
<tr>
<td>IO Pin</td>
<td>1 10 × 1</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Analogue Pin</td>
<td>0.001 10 × 1</td>
<td>0.01</td>
<td></td>
</tr>
<tr>
<td>TOTAL</td>
<td>490 µA / 914 uA</td>
<td>1.617 mW / 3.017 mW</td>
<td></td>
</tr>
</tbody>
</table>

The final system would eventually operate at 2.8 V instead of the 3.3 V, improving on the estimated power consumption above.

Therefore, the MCU power consumption was estimated to range between 1.3 mW and 1.7 mW as opposed to the original 600 mW of the MNM MCU.

High voltage supply

As shown by Fuchs [1], the NM requires a high voltage supply. The MNM was designed to support either a $^3$He or a $^{10}$BF$_3$ proportional counter tube. Thus, it was decided to change the high-voltage supply from a fixed voltage design to that of a digitally programmable supply to allow dynamic configuration of the high voltage and thereby ensure compatibility with $^{10}$BF$_3$ (900-1 100 V) or the $^3$He (1 200-1 350 V) proportional counter tubes.

The original MNM high-voltage supply also lacked low-temperature and low-power characteristics required by the new design. A suitable replacement supply was found, namely an EMCO ULP-20T. To evaluate the new module, Table 5-6 was drawn up to show a comparison of existing and new characteristics.
Table 5-6 High voltage component selection

<table>
<thead>
<tr>
<th>Specifications</th>
<th>Spellman MM5 1.5W</th>
<th>EMCO ULP-20T</th>
<th>Improvements</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>0 to 50 °C</td>
<td>-55 to 85°C</td>
<td>Industrial temperature</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>operation</td>
</tr>
<tr>
<td>Voltage</td>
<td>0 to 12 V</td>
<td>5.4 to 7.4 V</td>
<td>40 × Improved</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>power consumption</td>
</tr>
<tr>
<td>Power</td>
<td>80 mW</td>
<td>2 mW</td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>55 to 70%</td>
<td>&gt;85%</td>
<td></td>
</tr>
<tr>
<td>Size (mm)</td>
<td>50.0 × 50.0 × 30.0</td>
<td>83.8 × 38.1 × 12.7</td>
<td>Reduced volume</td>
</tr>
<tr>
<td>Volume</td>
<td>75 × 10⁻⁶ m³</td>
<td>40.5 × 10⁻⁶ m³</td>
<td></td>
</tr>
<tr>
<td>Surface</td>
<td>0.011 m²</td>
<td>0.009 m²</td>
<td></td>
</tr>
<tr>
<td>EMI</td>
<td>200kHz</td>
<td>1 Pulse / 4s</td>
<td></td>
</tr>
<tr>
<td>Voltage programming</td>
<td>Through supply</td>
<td>Dedicated programing</td>
<td></td>
</tr>
<tr>
<td>Output reference</td>
<td>No</td>
<td>Yes</td>
<td>Built-in reference</td>
</tr>
<tr>
<td>voltage</td>
<td></td>
<td></td>
<td>voltage</td>
</tr>
<tr>
<td>Internal HV</td>
<td>No</td>
<td>Yes</td>
<td>Built-in HV</td>
</tr>
<tr>
<td>measurement</td>
<td></td>
<td></td>
<td>measurement</td>
</tr>
</tbody>
</table>

A basic control loop was implemented to ensure a correct output voltage is provided by comparing the actual high-voltage output (divided to a lower value) with a reference value also provided by the high-voltage supply - this configuration is shown in Figure 5-7:

Figure 5-6 High-voltage architecture

Because the counter requires a constant high voltage, the static power consumption for this configuration was estimated as shown in Table 5-7:

Table 5-7 High voltage power budget

<table>
<thead>
<tr>
<th>Module</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULP-20T</td>
<td>Standard operation</td>
</tr>
<tr>
<td>DAC DAC8411</td>
<td>Standard operation</td>
</tr>
<tr>
<td>Total</td>
<td></td>
</tr>
</tbody>
</table>

Pre-amplifier

The amplifier of the data capturing sub-system comprises three main functions.
The MNM made use of three cascaded operational amplifiers to achieve these three functions. A fourth amplifier was combined with a resistive voltage divider for use as a voltage reference circuit in the MNM design. The MNM made use of a quad operational amplifier - the LF347 - which did not provide low power and low temperature characteristics. As shown in Table 5-8, three alternate op-amps were evaluated alongside the original:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>TSV71x series</th>
<th>MAX44248</th>
<th>LM158W</th>
<th>MNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>1.5 to 5.5 V</td>
<td>40 V</td>
<td>32 V</td>
<td>1.5 to 36 V</td>
</tr>
<tr>
<td>Temperature</td>
<td>-40 to 125 °C</td>
<td>-40 to 125 °C</td>
<td>-55 to 125 °C</td>
<td>0 to 70 °C</td>
</tr>
<tr>
<td>Current</td>
<td>0.016 mA / amp</td>
<td>0.09 mA / amp</td>
<td>0.3 mA / amp</td>
<td>2.75 mA / amp</td>
</tr>
<tr>
<td>GBW</td>
<td>150 kHz</td>
<td>1.0 MHz</td>
<td>1.1MHz</td>
<td>3 MHz</td>
</tr>
<tr>
<td>input bias</td>
<td>1 pA</td>
<td>150 pA</td>
<td>20 nA</td>
<td>50 pA</td>
</tr>
</tbody>
</table>

The selection of the new operational amplifier was based on operating voltage, individual amplifier operating current and individual input bias current. Of the operational amplifiers listed above, the TSV71x range was found to be the best suited for low-power and low temperature applications.

The MNM preamp configuration was changed to the configuration shown in Figure 5-8.

The pre-amplifier design was modified as follows:

1. A dedicated nano-power voltage reference IC (ISL21080), was used instead of a voltage divider network, improving temperature stability and reducing both power consumption and power supply related noise;

2. The original MNM required rejection of switching noise generated by the original Spellman high-voltage supply. Because the high voltage was changed to the ULP-20T, the switching noise at a fixed frequency was reduced to noise pulses every few seconds. This reduced the need for active filtering which also reduced the component count;

3. Lastly, an additional operational amplifier was incorporated into the pulse amplifier design. This improved the sensitivity of the pre-amplifier, resulting in improved pulse shaping.

Other than these minor adaptations, the pre-amplifier design remained functionally and physically the same as that of the MNM. In terms of performance, the new pre-amplifier provided improved power consumption and sensitivity.
Figure 5-8 Pre-amplifier design

The preamplifier is always on, making this device a static power consumer, as shown below:

Table 5-9 Pre-amplifier power budget

<table>
<thead>
<tr>
<th>Module</th>
<th>Power consumption</th>
</tr>
</thead>
<tbody>
<tr>
<td>TSV71x</td>
<td>0.211 mW</td>
</tr>
<tr>
<td>ISL21080 ($V_{REF}$)</td>
<td>0.005 mW</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td><strong>0.216 mW</strong></td>
</tr>
</tbody>
</table>

Real-time and location Unit

The MNM made use of an inexpensive GPS module to accurately synchronize the system’s time and location. Although the MNM GPS was found to adhere to the low-temperature requirements, the previous module was found to be a consumer of significant energy, thus an alternate component was acquired. Table 5-10 shows the comparison of the existing and newer generation GPS module:

Table 5-10 U-Blox GNSS/GPS module comparisons

<table>
<thead>
<tr>
<th>Parameters</th>
<th>LPT-NM</th>
<th>MNM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage</td>
<td>1.65 to 3.6V</td>
<td>2.7 to 3.6V</td>
</tr>
<tr>
<td>Temperature</td>
<td>-40 to 85 °C</td>
<td>-40 to 85 °C</td>
</tr>
<tr>
<td>Acquisition Current</td>
<td>22 mA</td>
<td>47 mA</td>
</tr>
<tr>
<td>Tracking (1 Hz)</td>
<td>5 mA</td>
<td>12 mA</td>
</tr>
<tr>
<td>Accuracy Time</td>
<td>100 ns</td>
<td>&lt; 60 ns</td>
</tr>
<tr>
<td>Size (mm)</td>
<td>16 × 12</td>
<td>22 × 17</td>
</tr>
<tr>
<td>Interface</td>
<td>USART/TTL</td>
<td>USART/TTL</td>
</tr>
<tr>
<td>Power consumption</td>
<td>79.2 mW</td>
<td>169.2 mW</td>
</tr>
</tbody>
</table>
The newer version of U-Blox module was found to have improved power ratings when compared to the previous module. Nonetheless, power consumption for the new module was still very high. For this reason, a power isolation switch was added to allow the MCU to electrically disconnect the GPS module power.

Because of the stationary environment in which the LPT-MNM will be used, the GPS module will only need an once-off location lock when it is initialized.

A timekeeping function was primarily used to correct clock drift of the MCU RTCC module. Because the MCU is rated to have a drift less than 3 s per month, with GNSS/GPS time lock occurring in less than one minute intervals, a single correction was required once daily.

Assuming that the system is allowed update its RTCC once per day, the power consumption for the GNSS/GPS module can be reduced to:

<table>
<thead>
<tr>
<th>Module</th>
<th>Power consumption mW</th>
</tr>
</thead>
<tbody>
<tr>
<td>NEO7-M GNSS module</td>
<td>61</td>
</tr>
<tr>
<td>MIC94060 High side power switch</td>
<td>0.006</td>
</tr>
<tr>
<td>Averaged cycled power</td>
<td>0.048</td>
</tr>
</tbody>
</table>

Temperature Sensor

It was shown in Section 3.13, that the counter tubes are sensitive to temperature fluctuations. The thermistor sensor previously used with the MNM was changed to a digital temperature sensor. The first reason for this decision was to improve accuracy of temperature measurements and secondly to remove the need for an additional ADC with its associated MCU code and power consumption.

As shown Table 5-12, a simple I2C interface temperature sensor was found with suitable characteristics.
Table 5-12 Temperature Sensors

<table>
<thead>
<tr>
<th>Parameters</th>
<th>MCP9804</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>-40 to 125 °C</td>
</tr>
<tr>
<td>Voltage</td>
<td>2.7 to 5.5V</td>
</tr>
<tr>
<td>Operating Current</td>
<td>200 μA</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>0.1 μA</td>
</tr>
<tr>
<td>Accuracy</td>
<td>±0.25 °C</td>
</tr>
<tr>
<td>Alarm pin out</td>
<td>Yes</td>
</tr>
<tr>
<td>Interface</td>
<td>I2C</td>
</tr>
</tbody>
</table>

Based on a cycle of one sample per minute, the average power consumption was calculated to be 0.009 mW.

Atmospheric pressure sensor

A second factor, other than temperature, that influences the neutron count rate is atmospheric depth as described in Section 1.3.2., which requires a digital barometer for pressure sensing. Two atmospheric pressure sensors used by the CSR were compared as shown in Table 5-13.

Table 5-13 Digital atmospheric pressure sensor

<table>
<thead>
<tr>
<th></th>
<th>Paroscientific Series 6 000</th>
<th>Vaisala PTB210</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>-54 to 60 °C</td>
<td>-40 to 60 °C</td>
</tr>
<tr>
<td>Voltage</td>
<td>6 to 16 V</td>
<td>5 to 28 V</td>
</tr>
<tr>
<td>Operating Current</td>
<td>16.5 mA</td>
<td>15 mA</td>
</tr>
<tr>
<td>Power down Current</td>
<td>7.0 mA</td>
<td>0.8 mA</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>N/A</td>
<td>0.2 mA</td>
</tr>
<tr>
<td>Interface</td>
<td>RS-232/ RS-485</td>
<td>RS-232 / TTL</td>
</tr>
</tbody>
</table>

Both sensors were found to satisfy the low-temperature requirements. The Vaisala sensor did however show two specific low-power benefits. The first being a slightly lower power consumption and a substantially lower sleep/idle power. The second benefit was that of a simplistic, low-voltage physical layer in the interface. The Paroscientific sensor required implementation of an RS232 level converter, increasing both circuit complexity and power consumption, while the Vaisala was available in a USART/TTL model, reducing the need for external components.

Because of increasing cost, the CSR has been systematically phasing out the use of the Paroscientific barometer. As a replacement, the CSR started using the less expensive Vaisala PTV210 barometer. The expense of this component and availability of existing stock limited the selection of pressure sensors to these two modules only.

Based on a cycle of one second samples, every 10 minutes the average power consumption was estimated to be 0.155 mW.

Data storage

The second highest consumer of power was determined to be the data storage module. The MNM used an Ethernet connection for transmitting data and a USB thumb drive as a backup
in the event of network failure. In the case of the LP-NM, the USB thumb drive was changed to an MMC/SD card. The characteristics are as follows:

<table>
<thead>
<tr>
<th></th>
<th>USB</th>
<th>MMC/SD</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>-40 to 60°C</td>
<td>-40 to 60°C</td>
</tr>
<tr>
<td>Voltage</td>
<td>5 V</td>
<td>2.7 to 3.6 V</td>
</tr>
<tr>
<td>R/W Current</td>
<td>75 mA</td>
<td>47 mA</td>
</tr>
<tr>
<td>Interface</td>
<td>USB</td>
<td>SPI/TTL</td>
</tr>
</tbody>
</table>

While the current consumption of MMC/SD is slightly lower than that of USB, the main power saving was based on the type of interface required. USB has increased code complexity and communicates constantly with almost double the operating voltage when compared to MMC/SD that uses SPI/TTL with reduced code complexity and less frequent communication.

With data written once every 30 minutes, the power consumption of a MMC/SD card was estimated at 0.094 mW.

**Computer interface**

Due to the autonomous nature of the new LP-NM system, there was no need to have an external, physical end-user interface. However, to facilitate debugging of the system, a USB serial interface was implemented to allow a developer to interact during development.

To ensure this additional feature does not affect the low-power performance of the system, the USB interface was implemented using a USB powered serial converter IC that is supplied with power from the 5 V USB VBUS interface from a monitoring PC, as shown in Figure 5-10.

**Figure 5-10 USB interface configuration**

The USB interface thus allows interfacing to the system in addition to the data storage card.

**Heating system**

Thus far, the design has focused on low-power only, but an additional function of the LPT-NM is internal heating, specifically when used at extremely low temperatures. Total active power consumption has been limited to less than 10 mW without the heating function. From Section
5.2.2 it was established that at least 350 mW would be required to heat the system 40 °C above ambient temperature, which implied a heating element. To accomplish this task, a digitally controlled resistor network was added to the system, as shown in Figure 5-11.

![Figure 5-11 Heating system](image)

A closed loop temperature control was implemented by using the resistive element and temperature sensor to ensure an acceptable internal operating temperature.

**Power management**

This section discussed the design of the power distribution network. Because each functional unit has its own unique voltage requirement, three different operating ranges were identified as shown below:

<table>
<thead>
<tr>
<th>High voltage</th>
<th>Mid voltage</th>
<th>Low voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>900 – 1,450 V</td>
<td>5.5 – 12 V Barometric pressure sensor</td>
<td>2.7 – 5 V Temperature sensor</td>
</tr>
<tr>
<td>Unspecified</td>
<td>6 – 7.5 V High Voltage (module supply voltage)</td>
<td>2.7 – 3.6 V GNSS time / location</td>
</tr>
<tr>
<td>Unspecified</td>
<td>2.7 – 3.6 V Pre-amplifier</td>
<td>1.8 – 3.6 V MCC/SD storage</td>
</tr>
</tbody>
</table>

![Figure 5-12 System operating voltages](image)
The NM counter requires a voltage of between 900 to 1 450 V as provided by a commercial high-voltage module. The remainder of the system requires mid and low voltage supplies.

Because the heating system did not form part of the electronic design as such but rather part of the electro-mechanical design, it was excluded from this section and will be discussed later.

Based on the lower limits of both mid and low-range voltage devices, it was decided to utilize two voltage levels of 6.1 V and 2.8 V. By keeping voltages to a minimum, power consumption was limited as discussed in Section 4.3.

DC-to-DC converters were used to transform voltages to required levels. Figure 5-13 shows the simplified system network configuration that was used.

![Figure 5-13 Simplified system power supply](image)

**Battery configuration**

Section 4.4.2 showed that lithium-thionyl chloride batteries are high capacity primary batteries ideal for use in low-temperature environments. A system power budget was required as shown in Table 5-15, which shows the system’s theoretical power consumption determined from design characteristics.

<table>
<thead>
<tr>
<th>Subsystem</th>
<th>Peak power (mW)</th>
<th>Device active duty cycle</th>
<th>Average power (mW)</th>
<th>Power per year (Wh)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU (12 MIPS)</td>
<td>11.03</td>
<td>0.74</td>
<td>1.48</td>
<td>12.9</td>
</tr>
<tr>
<td>MMC/SD</td>
<td>131.6</td>
<td>0.01</td>
<td>1.3</td>
<td>11.5</td>
</tr>
<tr>
<td>GNSS/GPS</td>
<td>61.6</td>
<td>0.005</td>
<td>0.308</td>
<td>2.7</td>
</tr>
<tr>
<td>Amplifier</td>
<td>0.196</td>
<td>1</td>
<td>0.196</td>
<td>1.7</td>
</tr>
<tr>
<td>High voltage supply</td>
<td>2.44</td>
<td>1</td>
<td>2.440</td>
<td>21.4</td>
</tr>
</tbody>
</table>
From this table, the power consumption was estimated to be between an average of 12.03 mW and a peak power of 298.9 mW. With a 3.6 V lithium-thionyl chloride battery, the expected load current would be in the range of 1.75 mA to 83.03 mA.

With the average power consumption shown in Table 5-15, the system would consume total of 54.32 Wh per year. A Tadiran SL-2790 battery was selected for its high capacity of 120 Wh at low temperatures.

However, because low temperature operation de-rates batteries, the de-rated values had to be used in battery capacity calculations. For the SL-2790 battery, operating at a load current of 1 to 100 mA and temperature of -40 °C, the de-rated specifications are:

**Table 5-16 Single cell Li/SOCl₂ temperature de-rating at -40 °C**

<table>
<thead>
<tr>
<th>Load current mA</th>
<th>Capacity Wh</th>
<th>Operating voltage V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>86</td>
<td>3.2</td>
</tr>
<tr>
<td>10</td>
<td>62</td>
<td>3.1</td>
</tr>
<tr>
<td>50</td>
<td>40</td>
<td>2.7</td>
</tr>
<tr>
<td>100</td>
<td>25</td>
<td>2.5</td>
</tr>
</tbody>
</table>

With a system operating between 1.45 and 83.03 mA, a lithium-thionyl chloride battery is thus expected to have a de-rated capacity of 46 to 72 % of its nominal capacity and an output voltage between 2.6 to 3.1 V. Assuming a worst-case capacity of 25 Wh and additional unaccounted-for losses, at least three batteries would be required to operate the data acquisition system.

Because batteries are more efficient at lower currents; a step-down converter design was selected. Figure 5-14 shows a series-cell battery pack making use of an efficient step-down regulator configuration. In doing so, the load current was lowered and battery capacity increased.

![Figure 5-14 System battery configuration](image-url)
An unaccounted system loss to be considered is DC-DC converter loss. Using a commonly available 80% efficiency step-down converter, system power consumption is increased by a factor of 1.25, which increases the total capacity requirement to 68.8 Wh per year, which still falls below the available capacity of the three-cell configuration.

**Heating module**

All previous designs were based on the assumption that the system was operating above a -40 °C operating temperature. To design for temperatures below -40 °C, a heating system was included as discussed earlier. The heating system was assigned its own battery pack to supply sufficient power for heating purposes. To reduce the total capacity requirement of these batteries, a photo-voltaic panel was added to the system.

![Heating module power network](image)

**Figure 5-15 Heating module power network**

Both battery and solar cells voltages were regulated and channelled to the heating network. The LPT-NM MCU was designed to monitor the system’s internal temperature and digitally control the heating elements. A simplistic on/off switching method was determined to be sufficient for this purpose.

A temperature model in Section 5.3.3 will determine the required battery capacity for internal heating, discussed under the topic of mechanical design.

**Circuit boards**

The complete system was integrated onto PCB modules as shown earlier. The design was kept as small as possible since, by reducing the enclosed volume, less energy is required to keep the enclosed volume heated. Also, by reducing the size of the individual boards, the effect of thermal expansion was mitigated, which reduced stresses on solder joints on modules.

As shown in Figure 5-16, different PCB modules were defined to allow for individual characterisation of each module during development and to allow for module swap-out when repairs are done.
By interconnecting modules using board-to-board connectors, modules could be easily changed, resigned and swapped out during development. This reduced the number of design cycles and the overall cost of development.

### 5.3.2 Software design

This section focuses on the software-implemented power management strategies design for low-power operation of the system. The system configuration, as described by Figure 5-5, is fundamentally responsible for:

- Detecting pulses;
- Accurate time-keeping;
- Sampling sensors:
  - Temperature measurements;
  - Barometric pressure measurements;
  - GNSS/GPS time and location updating;
- Moving data to a data storage device;
- System power management:
  - Task scheduling;
  - Battery monitoring;
- System protection:
  - Heating control.

The primary function of the system is to capture neutron particle events. Not surprisingly, this function was determined to be the function that had the biggest impact on power consumption. The MCU running in a conservative idle state consumes 26.9 Wh per year, almost half the total capacity shown earlier. By running the MCU mostly in a sleep mode reduced MCU power consumption to an estimated 1.9 Wh.

To implement sleep mode, a modified configuration of the previous MNM pulse capturing was needed as shown in Figure 5-18.
The modified configuration made use of one of the MCU’s internal asynchronous counters to log pulses. Due to the pulse shape of the pulses from the pre-amplifier that is connected to the counter tube, a comparator was required to digitise pulses. These pulses were routed to an internal counter that is able to count without executing code on the MCU, resulting in a significant energy saving as discussed above.

Looping back the comparator output directly into the counter input would have been sufficient, but the new high-voltage module was found to have a periodic noise that needed to be filtered out. A delay filter was added to the loop-back connection reducing the effect of the module noise.

Using the above configuration made it possible to keep the MCU in a constant sleep-mode state. The MCU therefore only wakes up when the counter’s register must be stored to memory or when a specified time has elapsed.

The process of data capturing is described in the following diagram that shows the three operating modes that were used.
In sleep-mode, the system active functional units were reduced to the real-time clock, comparator, watchdog timer and brownout detector. This placed the MCU in the lowest power consumption mode possible.

In low-speed mode all peripheral functions are available and MCU code resumes execution as shown in the figure above. By running at 10% of maximum clock speed, power consumption is still kept relatively low, a low-speed period during which dormant peripherals and sensors are activated and data collected.

All sensors are not sampled at the same rate. Modules such as the barometric pressure and GNSS/GPS are sampled at a fraction of the rate of the temperature sensor, for example. A task scheduler was used to set sample intervals according to sensor type and event type.

When the telemetric buffer is full, a write-to-memory procedure is executed. The MCU switches to high-speed mode to move buffered telemetric and counter data to the mass storage device as quickly as possible. After a data transfer, the MCU returns to sleep-mode and continues the counting neutron pulse events.

### Table 5-17 Scheduler tasks

<table>
<thead>
<tr>
<th>Function</th>
<th>Task</th>
<th>Interval</th>
<th>Active time (s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td>Sample temperature</td>
<td>1 / min</td>
<td>0.5</td>
</tr>
<tr>
<td>Power management</td>
<td>Sample battery voltages, estimate battery drain</td>
<td>1 / min</td>
<td>0.01</td>
</tr>
<tr>
<td>Heating management</td>
<td>Activate/de-activate heating system</td>
<td>1 / min</td>
<td>0.01</td>
</tr>
<tr>
<td>NM sample register</td>
<td>Move register to buffer</td>
<td>1 / min</td>
<td>0.01</td>
</tr>
<tr>
<td>Barometric pressure</td>
<td>Sample barometric pressure</td>
<td>1 / 30 min</td>
<td>4</td>
</tr>
<tr>
<td>Date/time</td>
<td>Synchronize the system RTCC</td>
<td>1 / day</td>
<td>60</td>
</tr>
<tr>
<td>Data storage</td>
<td>Move volatile memory to MMC/SD</td>
<td>1/30 min</td>
<td>0.01</td>
</tr>
</tbody>
</table>
All the peripheral modules have settling times for a valid sample to be captured. The following diagram shows the expected power consumption for each mode with reference to MCU activities.

![Power Consumption Diagram](image)

**Figure 5-19 Process timing**

By using this task scheduling technique, the MCU power consumption was limited to 1.85 mW including the DC-DC converter.

**Autonomous operation**

Autonomous operation, in this context, implied that the final LPT-NM product must operate as a standalone unit in a remote area. This further implied that temperature fluctuations had to be addressed in electronic and mechanical designs. Electronics were designed to function at temperatures down to -40 °C, as discussed above. Below -40 °C, internal must be provided to prevent component damage. The LPT-NM was designed to continually sample the enclosure temperature and regulate this temperature within specified limits. Due to limited energy, the heating element should only be used for short periods of time to preserve and rest batteries.

In order to prevent damage to components, the LPT-NM was designed to shut down when attempts to regulate internal temperature fail and the internal temperature falls below -40 °C.

The following diagram shows the heating workflow.
One of the tasks in the main control loop is temperature control. A temperature measurement is made every minute, after which the MCU determines whether heating should be activated or discontinued.

The LPT-NM was designed to calculate battery consumption (charge flow) to determine if heating can be done or if the system electronics should shut down safely. Thus, in case of temperatures that fall below a maintainable heating range, the system preserves power by disabling all main functions, effectively shutting down the system. In this mode, temperature measurement is the only function that is periodically activated, waiting for valid operating conditions before resuming data logging.

Batteries are also protected at lower temperatures when operating in a safe-shutdown mode. Loading the batteries at very low temperatures significantly reduces their capacity, leading to eventual failure of the system.

Operation returns to normal when the environmental conditions return to acceptable levels.

5.3.3 Mechanical design

This section describes mechanical and thermal modelling of the LPT-NM enclosure. Although the mechanical design was separated from the initial electronic circuit design, mechanical and
electronic circuit designs must be considered concurrently as there are constant trade-offs and considerations as shown in the design flow below.

![Design Flow Diagram](image)

**Figure 5-21 Mechanical system design flow**

The detailed mechanical design fell outside the scope of this research as aspects such as ingress protection (IP) and robustness could be addressed by well-known mechanical design and PC board protection methods (such as conformal coating, for example). However, low temperature would directly affect the electronic circuits and had to be considered as part of the electronic design part as per Figure 5-3.

**Temperature model**

A theoretical deployment of the LPT-NM at the South Pole station was used to define the operational conditions under which the LPT-NM will need to function. As obtained from available weather data, the following annual mean temperatures and available solar power for the South-Pole are known, as shown in the figure below.
From this graph it can be seen that the mean temperature falls below -40 °C for eight months in a year, with solar energy available for six months. Therefore, heating energy will be required for six months at least. Section 5.2.2 showed that an MNM insulated with 200 mm VIP panels required 300 mW to stay heated. With reference to the modelling techniques used in Section 5.2.2 and with the resized LPT-NM volume, the LPT-NM system heating requirement was recalculated as shown below:

To fit all components including batteries, the enclosed volume was increased, increasing overall heating requirements as a result. The primary components responsible for increasing the enclosed volume are the SL-2790 lithium-thionyl chloride batteries.
To include at least 15 batteries, the dimensions were increased to 200 × 200 × 130 mm as shown in Figure 5-24. The enclosed components include the barometric pressure sensor, the data capturing unit and the battery bank as shown below:

![Figure 5-24 Inner enclosure model](image)

To accommodate the increased volume, a new model was determined that required 11.2 mW / °C energy. Combining the thermal power requirements with the available weather data as shown in Figure 5-22, the following power consumption graph was compiled:

![Figure 5-25 Heater power required each month at South Pole](image)

From the above analysis, it was determined that 12 × SL-2790 batteries would be sufficient to heat the enclosed volume.

**Mechanical model**

A conceptual mechanical design of the LPT-NM is shown in the following illustration.
As shown, the proposed LPT-NM should be enclosed with thermal insulation, consisting of four layers of VIP panelling, surrounded by expanded polystyrene (EPE).

The enclosure is weather-proofed by enclosing the insulation in a corrugated polycarbonate container. Water and UV resistant corrugated polycarbonate plastic was found to be inexpensive. Silicon gaskets seals on all the joints and holes should effectively protect the enclosures against ingress. The use of silicone glue is recommended to seal the seams and any joints within the enclosure.

Where the cables exit the enclosure, closed cell silicone sponge rubber was found to be the best suited to provide water and airtight sealing of any gaps.

Because of the logistics in moving a large insulated container and due to the impracticality of heating the large counter body, the system was divided into two separate boxes. This allows the system to be easily transported using standard 800 × 800 mm pallets as shown in Figure 5-27. A 3D model of the system is shown in Figure 5-27.
From the model above it can be seen that the LPT-NM acquisition unit is accessible via an access panel on the side of the enclosure. This is the only point where ingress and thermal leakage might occur – a panel overlap and insert into the access hole should address this challenge.

5.4 Summary

From the problem statement and requirements of Section 3.4, three design aspects were addressed in this chapter:

1. A physical electronic device was designed using low-temperature (Section 4.3) and low-power (Section 4.4) components. This addressed the need for robustness and low power consumption. The design specifications were verified by means of experimental testing (to be presented in Section 6.2);

2. Along with the electronic design, the implementation of MCU firmware (Section 4.4.2) for the purpose of low-power consumption was developed. This firmware made use of the MCU power saving features to minimize consumption. To manage the de-rating of the battery bank capacity, the MCU was also made responsible for the enclosure internal environmental control to manage the internal temperature;

3. Finally, the complete system mechanical design was delivered as a meta-artefact in the form of a theoretical design (Figure 5-26) and a 3D simulated model (Figure 5-27). Due to a limited budget and a limitation in scope, the design had to be kept conceptual. A thermal conduction model (Figure 5-23) was provided to justify the design decisions – this serves as validation for the theoretical model.
6 System integration

6.1 Introduction

In addition to development methods and theoretical models to be delivered as met-artefacts, synthesis of the physical data acquisition unit was done to provide an artefact. Synthesis of the data acquisition unit (MN-DAS) was completed in the three steps, as outlined in the following sections.

6.1.1 Computer aided model design

The first phase of the design was computer aided modelling of the LPT-NM data acquisition unit. The circuit designs presented in Appendix ABC were used as logical designs from which to construct printed circuit boards.

The data acquisition unit was divided into four modular circuit boards. From the circuit layouts, 3D models of these four modules were created as shown in Figure 6-1. The pre-amplifier board was enclosed in a shielded housing to prevent high voltage coupling and other sources of external noise from interfering with measurements.

![Figure 6-1 PCB 3D CAD model](image)

The purpose of the 3D model was for to assist with mechanical design. The dimensions of the printed circuit boards defined the internal space required and provided the inner dimensions of the mechanical enclosure.

Physical constructs were thus realised in the DSR sense for test and evaluation purposes.

6.1.2 Circuits designs

The logical design, as specified in Section 5.3.1, was thus implemented using components selected for low temperature (discussed in Section 4.3.2) and low power (discussed in Section 4.4.1). The following set of PCB’s was manufactured, as discussed below.
The MCU module shown above was kept to a minimum size and complexity. The on-board features were limited to GPS, USB, temperature measurement and data storage.

The modularity of the MCU and peripheral boards allowed evaluation of individual board functionality and performance – thus allowed individual characterisation of each module.

**Figure 6-2 MCU board**

The power-distribution module was made to slot into the MCU module as indicated in Figure 6-4. This design went through multiple iterations to find a suitable DC/DC converter before a final physical form resulted.

**Figure 6-3 Power distribution board**
The high voltage module was found to be the most expensive component of the data acquisition unit. Therefore, the circuit layout was kept simplistic to avoid costly iterations, which resulted in the pre-amplifier module being implemented on a smaller board that could be slotted into the larger high-voltage supply board. Prior research showed that the pre-amplifier design was susceptible to environmental electromagnetic noise, thus the pre-amplifier required a shielding enclosure to minimize electromagnetic interference.

The high-voltage module was made to slot into both the power-distribution and MCU module boards.

A programming interface was added onto the high-voltage module to allow in-system programming of the MCU. A pre-amplifier test point was also added as shown in Figure 6-4.

### 6.1.3 Final constructed data acquisition unit assembly

Figure 6-5 shows the final physical configuration of the data acquisition unit.
6.1.4 Cost assessment

Although cost was considered a research challenge, the electronic development cost compared to the NM counter assembly was found to be minimal.

Table 6-1 shows the relative cost of the electronic components within the design.

<table>
<thead>
<tr>
<th>Modules</th>
<th>Percentage of total cost</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU</td>
<td>1 %</td>
</tr>
<tr>
<td>Power-distribution</td>
<td>1 %</td>
</tr>
<tr>
<td>Amplifier</td>
<td>1 %</td>
</tr>
<tr>
<td>High voltage</td>
<td>8 %</td>
</tr>
<tr>
<td>Battery bank</td>
<td>6 %</td>
</tr>
<tr>
<td>Pressure sensor</td>
<td>30 %</td>
</tr>
<tr>
<td>NM-Counter</td>
<td>53 %</td>
</tr>
</tbody>
</table>

The two most expensive components, of which alternatives are as yet unavailable, accounted for 83 % of the total cost. The batteries including the heating module’s batteries, made up an additional 6 %.

The electronic design only made up 11 % of the total design, of which cost was estimated for a single production unit. By producing multiple units, it could be reduced even further.

6.2 Empirical tests and results

Following the DSR guidelines shown in Section 2.4, the utility of the electronic construct had to be evaluated through rigorous experimental verification. Thus LPT-NM had to be measured determining its characteristics along with any limitations within the design.
6.2.1 Experiment 1: Functional capability assessment

Purpose

The capability of the LPT-NM unit was verified by testing each individual function.

Experimental setup

To facilitate the testing of each function, separate firmware was developed to test each subsystem’s functional capability. Each function was evaluated on a go/no-go basis.

Experimental method

**Step 1:** All boards were tested for manufacturing defects by testing the continuity of signal paths and the presence of short-circuits. This was done to prevent damage to modules when they were powered-up for the first time.

**Step 2:** Boards were connected to a bench power-supply and individually powered up. All the appropriate voltages on the modules were verified by testing the appropriate supply lines with a meter. The initial design decision to follow a modular design assisted this step significantly.

**Step 3:** After all elements on the board were tested electrically, boards were combined into a single unit and powered up, testing the supply line once more.

**Step 4:** Because the LPT-NM is an MCU controlled system, it was necessary to develop firmware and drivers for each individual function. Firmware was therefore developed.

**Step 5:** Firmware was loaded onto the MCU and each function enabled individually. Based on the required function, each process and output of that function was measured to determine whether firmware was indeed executing the task required.

**Step 6:** Step 5 was repeated for all the required tasks as indicated in and recoded in Table 6-2.

Acceptance criteria

Throughout this test procedure, voltages were constantly measured to validate electrical characteristics of all modules. The digitally controlled functions were validated by their respective output functions.

Measured results

Based on the design (discussed in Section 6.1.2) and the functional requirements (shown in Figure 5-5) the following list of LPT-NM functional were tested as shown in Table 6-2.
### Table 6-2 Functional units tested

<table>
<thead>
<tr>
<th>Function</th>
<th>Tested</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Power supply functions</strong></td>
<td></td>
</tr>
<tr>
<td>Programmable 900-1500 V high-voltage supply</td>
<td>✓</td>
</tr>
<tr>
<td>Fixed 2.8 V power supply</td>
<td>✓</td>
</tr>
<tr>
<td>Fixed 6.1 V power supply</td>
<td>✓</td>
</tr>
<tr>
<td><strong>NM counter functions</strong></td>
<td></td>
</tr>
<tr>
<td>NM counter pulse amplification</td>
<td>✓</td>
</tr>
<tr>
<td>NM pulse detection by a comparator</td>
<td>✓</td>
</tr>
<tr>
<td>Minute average pulse counting</td>
<td>✓</td>
</tr>
<tr>
<td><strong>Environmental sensor functions</strong></td>
<td></td>
</tr>
<tr>
<td>GPS/GNSS time/location capturing</td>
<td>✓</td>
</tr>
<tr>
<td>Atmospheric pressure capturing</td>
<td>✓</td>
</tr>
<tr>
<td>Ambient temperature capturing</td>
<td>✓</td>
</tr>
<tr>
<td><strong>Data management functions</strong></td>
<td></td>
</tr>
<tr>
<td>MMC/SD data storage</td>
<td>✓</td>
</tr>
<tr>
<td>Computer USB interface</td>
<td>✓</td>
</tr>
<tr>
<td><strong>Power management functions</strong></td>
<td></td>
</tr>
<tr>
<td>High-voltage module voltage measurement</td>
<td>✓</td>
</tr>
<tr>
<td>Battery voltage measurement</td>
<td>✓</td>
</tr>
<tr>
<td>Heating network</td>
<td>✓</td>
</tr>
<tr>
<td><strong>MCU</strong></td>
<td></td>
</tr>
<tr>
<td>Real-time clock and calendar</td>
<td>✓</td>
</tr>
<tr>
<td>Sleep-mode NM counting</td>
<td>✓</td>
</tr>
<tr>
<td>Low-clock-speed sensor interfacing</td>
<td>✓</td>
</tr>
<tr>
<td>High-clock-speed data processing</td>
<td>✓</td>
</tr>
</tbody>
</table>

### Conclusion

Thus the LPT-NM construct was experimentally tested, proving that it is capable of fulfilling the functional requirements of a neutron monitor.

#### 6.2.2 Experiment 2: Task performance (time)

### Purpose

Because MCU activities are executed in a relatively short period of time, their power consumption could not be measured by means of a current shunt-resistor. Rather, an average power had to be measurement by use of a current discharge circuit.

However, before any power consumption measurements were undertaken, a measurement of the MCUs task execution times was needed. Thus an experiment to determine these times required for each task was set up.

### Experimental setup

Individual task periods were measured by having the MCU output a logical ‘1’ as a task was started, and to a logical ‘0’ as a task was completed. The generated pulse was then used to measure the task period.
Experimental method

Step 1: A list of tasks was compiled based on the functional requirements (shown in Figure 5-5).

Step 2: Using the MCU firmware that was developed for experiment 1, the firmware was set up to repeat a specific task every second, while producing its associated task-pulse.

Step 2: Functions were thus tested, by up-loading the firmware to the MCU and repeating the process for each individual task.

Step 3: Finally by using an oscilloscope’s, the task pulse width was measured and recoded in Table 6-3.

Measured results

<table>
<thead>
<tr>
<th>Task</th>
<th>MCU operating mode - clock speed</th>
<th>Task process time (ms)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Atmospheric pressure average wake-up time</td>
<td>None</td>
<td>2 000- 4 000</td>
</tr>
<tr>
<td>Temperature sensor average wake-up time</td>
<td>None</td>
<td>240-500</td>
</tr>
<tr>
<td>GNSS/GPS average time to satellite</td>
<td>None</td>
<td>29 000-60 000</td>
</tr>
<tr>
<td>acquisition</td>
<td></td>
<td></td>
</tr>
<tr>
<td>MCU wake-up/sleep</td>
<td>Low</td>
<td>&lt; 1</td>
</tr>
<tr>
<td>ADC sample voltage</td>
<td>Low</td>
<td>0.5</td>
</tr>
<tr>
<td>Temperature sensor sample</td>
<td>Low</td>
<td>1</td>
</tr>
<tr>
<td>Atmospheric pressure sample</td>
<td>Low</td>
<td>1</td>
</tr>
<tr>
<td>GNSS/GPS time/location sample</td>
<td>Low</td>
<td>10</td>
</tr>
<tr>
<td>MCU high speed wakeup</td>
<td>High</td>
<td>7.2</td>
</tr>
<tr>
<td>MCU move 512 bytes data</td>
<td>High</td>
<td>17.42</td>
</tr>
<tr>
<td>MMC/SD write data</td>
<td>High</td>
<td>147.2</td>
</tr>
<tr>
<td>MCU entering sleep</td>
<td>High</td>
<td>1.8</td>
</tr>
</tbody>
</table>

Conclusion

It is clear from the values above that the MCU takes milliseconds to process most tasks. The processes observed to take the most time were associated with acquiring data from three sensor modules. Each sensor required time to settle before any valid data could be captured.

Although sensor wake-up times ranged from 0.24 to 60 s, it was found that these times did not influence the MCU activity due to the fact that the MCU remained in sleep-mode whilst the sensors were waking up. It is only after a predefined period that the MCU wakes up and
resumes capturing samples from these sensors. With this configuration, the MCU does not need to be awake for the sensor wake-up period, saving power in the process.

To better understand the MCU task timing, three timing diagrams were compiled as shown in Appendix E.

Table 6-3 shows the time the MCU spends in either low-speed mode or high-speed mode. Any time other than these the MCU would effectively remain in sleep mode.

<table>
<thead>
<tr>
<th>Table 6-4 Combined MCU task performance</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>MCU sample task</strong></td>
</tr>
<tr>
<td>-------------------------------</td>
</tr>
<tr>
<td><strong>Low-speed mode</strong></td>
</tr>
<tr>
<td>NM-counter and temperature samples</td>
</tr>
<tr>
<td>Atmospheric pressure samples</td>
</tr>
<tr>
<td>Real time clock GPS/GNSS update</td>
</tr>
<tr>
<td><strong>High-speed mode</strong></td>
</tr>
<tr>
<td>Once per hour data write action</td>
</tr>
</tbody>
</table>

By using the task performance of Table 6-3, combined with the sensor sample rates, the annual task performance for the complete LPT-NM unit was shown to be:

<table>
<thead>
<tr>
<th>Table 6-5 Annual active time for module functions</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hours active per year (h/y)</strong></td>
</tr>
<tr>
<td><strong>MCU modes</strong></td>
</tr>
<tr>
<td>MCU Sleep</td>
</tr>
<tr>
<td>MCU low-clock-speed</td>
</tr>
<tr>
<td>MCU high-clock-speed</td>
</tr>
<tr>
<td><strong>Peripheral modules</strong></td>
</tr>
<tr>
<td>Temperature sensor</td>
</tr>
<tr>
<td>Atmospheric pressure sensor</td>
</tr>
<tr>
<td>GNSS/GPS module</td>
</tr>
<tr>
<td>MMC/SD memory card</td>
</tr>
<tr>
<td>Pre-amplifier</td>
</tr>
<tr>
<td>2.8 V power supply</td>
</tr>
<tr>
<td>6.1 V power supply</td>
</tr>
<tr>
<td>High-voltage supply</td>
</tr>
</tbody>
</table>
6.2.3 Experiment 3: Individual module power consumption

Purpose

The LPT-NM was designed to function with low power consumption. This theoretical consumption had to be verified through experimental testing. It was only through testing that the unit’s characteristic could be assessed.

Experimental setup

Power consumption was measured using a micro-power measurement experiment as discussed in Section 4.4.3. A fast-switching relay and microcontroller were used to measure the average power consumption of individual components, as shown in Figure 6-6.

![Micro-power measurement circuit](image)

**Figure 6-6 Micro-power measurement circuit**

(4.22 was used to calculate the average dynamic current consumption. The experiment was also verified using a known resistive load to calibrate the measurement for accuracy.

Experimental method

**Step 1:** The LPT-NM modules were disconnected from one another and connected to the measuring circuit separately.

**Step 2:** A bench power supply was used to provide the appropriate voltage to each module, powering the module indirectly through the experimental setup above.
**Step 3:** In order to measure all the functions controlled by the MCU module, it was necessary to first measure the MCU module’s base power consumption. For this, dedicated firmware was used to run the MCU in the three respective operating modes. While testing the MCU, no peripheral functions were activated, therefore isolating and determining the MCU power consumption in isolation.

**Step 4:** Using the firmware developed in Experiment 1, the MCU was used to activate individual peripherals.

**Step 5:** For each iteration of the test, the MCU and peripheral power consumptions were measured.

**Step 6:** Because the MCU had to be active to interface with the respective peripherals, the MCU consumption of Step 3 had to be subtracted from the results obtained in Step 5 in order to give individual peripheral power consumptions.

**Measured results**

Table 6-6 show the theoretical design specifications compared to the measured specifications.

<table>
<thead>
<tr>
<th>Device</th>
<th>Theoretical power consumption (mW)</th>
<th>Measured power consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU sleep mode + RTCC</td>
<td>0.05 – 0.08</td>
<td>0.5</td>
</tr>
<tr>
<td>MCU low-speed (1MIPS)</td>
<td>0.30 – 0.50</td>
<td>2.15</td>
</tr>
<tr>
<td>MCU high-speed (12MIPS)</td>
<td>7.40 – 17.4</td>
<td>13.96</td>
</tr>
<tr>
<td>Pre-amplifier</td>
<td>0.2</td>
<td>0.37</td>
</tr>
<tr>
<td>Pressure sensor</td>
<td>91</td>
<td>51.74</td>
</tr>
<tr>
<td>Temperature sensor</td>
<td>1.2</td>
<td>0.5</td>
</tr>
<tr>
<td>High voltage module</td>
<td>2.7</td>
<td>2.57</td>
</tr>
<tr>
<td>MCC/SD storage device</td>
<td>131.6</td>
<td>141</td>
</tr>
<tr>
<td>GNSS/GPS module</td>
<td>63.8</td>
<td>44.7</td>
</tr>
</tbody>
</table>

**Conclusion**

It is clear from Table 6-6, that the sub-milliwatt power consumption values showed a higher than expected measurement, as is seen from the first three entries in the table. These values were attributed to unexpected leakage currents in module circuits. Although these values were found to be higher than the predicted theoretical values, better than expected results were obtained from the higher-power consuming modules.

Overall, the measured result was found to be 51 mW less than the theoretically expected power consumption.
6.2.4 Experiment 4: Regulator module power consumption

Purpose

As was discussed in Section 5.3.1, DC to DC converters were used to power individual modules. For this reason, it was necessary to measure the regulators’ efficiency and any losses as a result thereof. The following experiment was conducted to show the power consumption of the regulators with the individual peripherals connected.

Experimental setup

Step 1: Using the micro-power measurement setup of Experiment 2, one of the voltage regulators was connected.

Step 2: The unloaded regulator power consumption was measured.

Step 3: The regulator was loaded with the individual peripheral circuits.

Step 4: The power consumption of the regulator was then measured for each of the specific peripherals.

Step 5: Each peripheral’s power consumption was thereafter calculated by subtracting the base regulator power consumption.

Step 6: The regulator efficiency was thus calculated by dividing the results obtained from Experiment 3 with the newly calculated consumptions results.

Step 7: Within the conclusion, the individually measured results were combined with that of the task performance results to yield an annual power budget.

Measured results

Table 6-7 shows the base power consumption of the two voltage regulators.

<table>
<thead>
<tr>
<th>DC/DC converter</th>
<th>Theoretical Consumption (mW)</th>
<th>Measured Consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.8 V buck converter</td>
<td>1.125</td>
<td>0.19</td>
</tr>
<tr>
<td>6.1 V buck converter</td>
<td>1.125</td>
<td>1.37</td>
</tr>
</tbody>
</table>
Table 6-8 Module power consumption via a DC/DC converter module measurement

<table>
<thead>
<tr>
<th>Device</th>
<th>Experiment 3 measured power consumption (mW)</th>
<th>Measured DC/DC power consumption (mW)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU sleep mode + RTCC</td>
<td>0.5</td>
<td>1.37</td>
</tr>
<tr>
<td>MCU low-speed (1MIPS)</td>
<td>2.68</td>
<td>2.86</td>
</tr>
<tr>
<td>MCU high-speed (12MIPS)</td>
<td>17.45</td>
<td>23.39</td>
</tr>
<tr>
<td>Pre-amplifier</td>
<td>0.46</td>
<td>0.42</td>
</tr>
<tr>
<td>Pressure sensor</td>
<td>64.68</td>
<td>51.25</td>
</tr>
<tr>
<td>Temperature sensor</td>
<td>0.63</td>
<td>0.77</td>
</tr>
<tr>
<td>High-voltage module</td>
<td>3.21</td>
<td>3.01</td>
</tr>
<tr>
<td>MMC/SD card</td>
<td>141</td>
<td>169.8</td>
</tr>
<tr>
<td>GNSS/GPS module</td>
<td>55.86</td>
<td>66.92</td>
</tr>
</tbody>
</table>

**Conclusion**

The sub-milliwatt power measurements provided results that showed higher consumption than expected. However, this was offset by the better than expected efficiency of the higher power consuming peripherals.

Using the values obtained in this experiment the annual power budget was calculated using the task execution times obtained from Experiment 2.

Table 6-9 Sleep-mode power consumption with DC/DC converter losses

<table>
<thead>
<tr>
<th>Device</th>
<th>Unit power consumption (mW)</th>
<th>H/y</th>
<th>Wh/y</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCU sleep</td>
<td>1.37</td>
<td>8 687</td>
<td>11.9</td>
</tr>
<tr>
<td>MCU low-speed</td>
<td>2.86</td>
<td>73</td>
<td>0.210</td>
</tr>
<tr>
<td>MCU high-speed</td>
<td>23.39</td>
<td>0.42</td>
<td>0.009</td>
</tr>
<tr>
<td>Pre-amplifier</td>
<td>0.42</td>
<td>8 760</td>
<td>3.679</td>
</tr>
<tr>
<td>Pressure sensor</td>
<td>51.25</td>
<td>19.5</td>
<td>0.999</td>
</tr>
<tr>
<td>Temperature sensor</td>
<td>0.77</td>
<td>73</td>
<td>0.056</td>
</tr>
<tr>
<td>MMC/SD card</td>
<td>169.8</td>
<td>0.36</td>
<td>0.061</td>
</tr>
<tr>
<td>GNSS/GPS module</td>
<td>66.92</td>
<td>6.08</td>
<td>0.407</td>
</tr>
<tr>
<td>2,8 V power supply</td>
<td>0.19</td>
<td>8760</td>
<td>1.664</td>
</tr>
<tr>
<td>6,1 V power supply</td>
<td>1.37</td>
<td>8760</td>
<td>12</td>
</tr>
<tr>
<td>High-voltage supply</td>
<td>3.01</td>
<td>8760</td>
<td>26.368</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td></td>
<td>57.36</td>
<td></td>
</tr>
</tbody>
</table>

The LPT-NM average power consumption was thus shown to be 6.5 mW, with an annual energy requirement of 57.35 Wh.

This result validated the original design decision of three lithium-thionyl chloride batteries (75 Wh) discussed in Section 5.3.1 and Table 5-16.
6.2.5 Experiment 5: Temperature performance

Purpose

The purpose of this experiment was to verify the operation of the LPT-NM at low-temperatures. The primary concern while operating the MCU in a low-temperature environment was the reliability of its crystal oscillator units.

Although the crystal oscillator units were selected with -40 °C specifications, the functional performance of the LPT-NM had to be verified.

Therefore the goal of this experiment was to establish whether the MCUs oscillators would fail to operate at temperatures exceeding their manufactures’ lower operating limit.

Experimental method

Step 1: Using dedicated firmware, the MCU module’s high-speed and low-speed crystal oscillators were configured to produce reference pulses to the board’s output ports. To monitor the MCU temperature, the module was also configured to take a temperature measurement every second.

Step 2: Using an oscilloscope, the reference pulses were monitored whilst temperature measurements were transmitted to an external PC using the modules’ USB interface.

Step 4: While the unit was capturing temperature samples, it was placed inside a -70 °C bio-refrigerator.

Step 5: The module was then allowed to cool from the ambient temperature of 20 °C down to the refrigerator temperature of -70 °C.

Step 6: The modules’ reference pulses were monitored for timing variance and failure. In case of failure, the temperature could be used as the critical operating temperature.

Step 7: To test the oscillator cold-start performance, the module was also powered down at -70 °C and allowed to cool down for a period of 5 minutes. Thereafter a cold-restart was attempted by replying power to the module.

Measured results

<table>
<thead>
<tr>
<th>Crystal</th>
<th>Operating temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>20 °C</td>
</tr>
<tr>
<td>32 kHz</td>
<td>✓</td>
</tr>
<tr>
<td>24.56 MHz</td>
<td>✓</td>
</tr>
<tr>
<td>MCU internal FRC</td>
<td>✓</td>
</tr>
</tbody>
</table>
Table 6-11 Crystal oscillator cold-start test

<table>
<thead>
<tr>
<th>Crystal</th>
<th>Started Ok</th>
<th>-40 °C</th>
<th>-70 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>32 kHz</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>24.56 MHz</td>
<td>✓</td>
<td>✓</td>
<td></td>
</tr>
<tr>
<td>MCU internal FRC</td>
<td>✓</td>
<td></td>
<td>×</td>
</tr>
</tbody>
</table>

Conclusion

Of all the oscillators, the MCU FRC was the only oscillator that failed to start at a -70 °C temperature. It was also found that the FRC frequency changed substantially as the temperature lowered, slowing down as the temperature decreased.

Therefore the unit was found to function at a temperature well below the manufacturers’ recommended operational limit. It can therefore be concluded that although this proves functionality at very low temperatures, without long term testing it must be assumed that the product life expectancy would most likely be reduced by thermal cycling stresses, according to theory.

6.3 Summary

The electronic design was verified by means of experimental testing to validate the physical construct (artefact) developed as part of this research.

- From the functional experiment, all the device functions were shown to be capable. This provided evidence that the unit is capable of performing all tasks as derived from the functional analysis;

- The tasks performance measurements showed that the MCU could be placed in a sleep state for 99 % of its operational time to provide better than estimated power consumption;

- The power consumption experiments showed the actual power consumption to be slightly higher than expected. However, the improved task performance eased this effect and kept total power consumption below an acceptable value;

- The last experiment tested the physical constructs’ electronic low-temperature tolerance. The modules were found to function to a temperature as low as -70 °C, with the exception of the MCUs internal FRC oscillator. Because the design implemented dedicated crystal oscillators, this shortfall had no material effect.

From the above mentioned results, it was thus concluded that the design satisfied functional, low-power and low-temperature performance requirements.
7 Validation and conclusion

This chapter concludes the research and design of a low-power low-temperature neutron monitor. The research problem was suggested by previous work done by Fuchs [1] and Kruger [2], who initiated the development of an autonomous neutron monitor.

Using the DSR research process, the maturity of this research was determined to be an improvement on an existing system. Thus, the challenges related to an improved design had to be determined whilst still keeping the original neutron monitor design constraints of size and cost in mind.

The improved monitor requires the deployment of such a monitor at geographical locations that lack infrastructure such as power and environmental protection. Using the preliminary literature review as a point of departure, the environmental constraints (discussed in Section 4.8) were identified to include the challenge of low-temperature operation, i.e.: design of electronics, materials and batteries for low temperature operation.

The monitor also has to function in an isolated remote location, leading to the additional research challenges of energy sources, low-power circuits, data storage and autonomous operation.

A final study into environmental protection had to be conducted because of the remote location, which also led to the definition of environmental constraints applicable to this application.

Using the DSR process’ rigor, the initial research problem was validated from knowledge presented in literature. The resulting solution was to research, design and test an electronic data acquisition unit (neutron counter with registration unit) and to provide a theoretical model for a mechanical enclosure (a low temperature model).

The data acquisition unit (Section 6.1.3) was designed and its functional performances tested and verified against the original requirements, as follows:

- Power consumption performance was measured and evaluated for low power operation;

- Low-temperature performance was measured using a -70 °C bio-refrigerator. The unit was found to function within the recommended operational limits; the experiment however did not address long-term reliability of the unit as this fell outside the scope of this research;

- The most expensive component within the neutron monitor was found to be the counter assembly, comprising the counter tube, reflector, producer and moderator. The electronic component cost was a fraction of the total unit cost and therefore was not considered a significant cost limitation.

The mechanical design was limited to a theoretical model due to the project budget.
- A temperature model was produced to show the unit’s internal temperature characteristics using the literature of Chapter 4;

- The mechanical enclosure heating requirement was modelled to show that a 300 mW heating load would be sufficient for a -65 °C ambient temperature;

- The logistic problem of transportability was addressed by the modular design of the enclosure to allow for transportation on a pallet;

- While developing the mechanical model, cost was always considered when selecting a solution. The design complexity was kept to a minimum by using simplicity as part of the design philosophy.

For validation of the design, the design requirements and their validation references are shown in Table 7-1 below:

### Table 7-1 Requirement validation summary

<table>
<thead>
<tr>
<th>User requirements</th>
<th>Addressed by the MMC/SD design in Figure 5-17</th>
</tr>
</thead>
<tbody>
<tr>
<td>Measuring cosmic-ray activity</td>
<td>Addressed by the MMC/SD design in Section 5.2</td>
</tr>
<tr>
<td>Measuring ambient temperature</td>
<td>Addressed by the MMC/SD design in Section 5.2</td>
</tr>
<tr>
<td>Measuring atmospheric pressure</td>
<td>Addressed by the MMC/SD design in Section 5.2</td>
</tr>
<tr>
<td>Internal data storage</td>
<td>Addressed by the MMC/SD design in Section 5.2</td>
</tr>
<tr>
<td>Independent power source</td>
<td>Addressed by the power management design in Figure 5-14.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Environmental requirements</th>
<th>Addressed by low-temperature components selection shown Section 4.2.2 and Section 5.2.1.</th>
</tr>
</thead>
<tbody>
<tr>
<td>-65 °C to +30 °C operating temperature</td>
<td>Temperature model Figure 5-23</td>
</tr>
<tr>
<td>Ingress protection</td>
<td>Addressed by seals selected in Section 4.7.2</td>
</tr>
<tr>
<td></td>
<td>Addressed by mechanical design model 5.2.3</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Performance requirements</th>
<th>Low-power component selection/ design of Section 5.2.1</th>
</tr>
</thead>
<tbody>
<tr>
<td>12 month operation</td>
<td>Low-power design validation</td>
</tr>
<tr>
<td></td>
<td>Battery selection Section 4.4 and Table 4-15</td>
</tr>
<tr>
<td></td>
<td>Power budget Table 5-15</td>
</tr>
<tr>
<td>1/min NM-counting sample rate</td>
<td>Software operating system design of Section 5.2.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Logistical requirements</th>
<th>Mechanical model shown in Figure 5-26</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size constraint</td>
<td>Pallet compatible design shown Figure 5-27</td>
</tr>
<tr>
<td>Transportable</td>
<td>Simplistic design philosophy</td>
</tr>
<tr>
<td>Cost constraint</td>
<td></td>
</tr>
</tbody>
</table>
7.1 Proposed future work

This thesis serves as a design reference for a low-temperature low-power neutron monitor in future development. However, electronic components are constantly changing. Advances in technology will potentially lead to new and more advanced components to be selected using the methods proposed in this thesis.

7.1.1 Theoretical mechanical modelling

A theoretical mechanical model was provided, and future work can be done to improve the quality of the mechanical design. Currently, the design makes use of pre-fabricated panelling to insulate and protect the electronic unit inside. Seams and joints are still subject to long-term mechanical fatigue that poses a reliability concern. Moulding a single-piece enclosure would reduce ingress risk, thermal leaks, and durability. Practical considerations must therefore be considered in future development.

7.1.2 Electronic reliability testing

In the proposed design, a heating module was added to ensure the electronic module enclosed temperature does not fall below the operational limit of -40 °C.

The low temperature operational test demonstrated that the modules could function at a temperature as low as -70 °C. In future work, an additional experiment must be performed to validate long-term operation at sub -40 °C temperatures.

Results from the proposed future experiment may lead to a reduction in the heating requirement, which could lead to an additional saving in cost and increase in reliability.

7.1.3 Alternate energy

Batteries were used as the primary form of energy to simplify the end product. To reduce cost and extend the monitor’s operational lifetime, alternative energy sources may be added to the design.

The literature reviewed available alternatives, but due to a reliability requirement at lower temperatures, these were excluded from the design. Advances in technology may provide future development opportunities for the project.
### 7.2 Validation matrix

#### Table 7-2. Research validation matrix

<table>
<thead>
<tr>
<th>Chapter 1</th>
<th>Cosmic ray physics</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Neutron monitor principles</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Future development challenges</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Chapter 3</td>
<td>Previous system CMN/ MMN</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Environmental observations</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Economic research environment</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Research challenges**

- Extreme environmental conditions/challenges
- Operation in remote locations
- Logistical constraints
- Limited budget

**Literature focus areas**

<table>
<thead>
<tr>
<th>Chapter 4</th>
<th>Thermal dynamics</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-temperature electronics Behaviour</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low-power circuit design</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Electronic energy/power sources</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data storage systems</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Environmental protection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Research solutions**

- Robust electronics
- Mechanical implementation
- Autonomous operation
- Design for transportability
- Low cost design

<table>
<thead>
<tr>
<th>Chapters 5 and 6</th>
<th>LPT-NM</th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal feasibility study</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Theoretical mechanical (design)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LP MNM DAS (construct)</td>
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<td>Power system design (method)</td>
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<td>Autonomous design (method)</td>
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<td>Design guide for future development (knowledge base)</td>
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<td>Specification of limitations and performance</td>
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<td>Documentation (knowledge base)</td>
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↑ Constructs  ↑ Model  ↑ Method  ↑ Knowledge base
The research validation matrix above is used to provide a combined view of this research. More specifically, the matrix provides the following:

- In the top section, the matrix shows the information sources used to validate the research problem and its associated challenges. Four research challenges were identified as shown in the matrix. The integrity of the information sources are used to validate the research problem. The “down” arrows in this section shows how information sources link to research challenges – these research challenges thus combine to describe the research problem;

- The middle section shows how research challenges were further investigated by using literature that specifically aligned six research topics with each research challenge. The matrix shows how the research challenges were systematically confirmed from literature by using “up” arrows. Also, literature added to the final solution by providing information to solve challenges as shown in the matrix, as shown by the “down” arrows;

- The bottom section shows how a solution was constructed from logical deduction and reasoning, creative input from combining existing solutions found from literature, electronic design input and implementation, and theoretical mechanical modelling. The final solution, namely the LPT-NM, addressed the initial real-world need by combining smaller solutions, also shown in the matrix by using “up” arrows. Colours were used to show how DSR outputs align with the smaller solutions.

From the matrix it becomes clear that the initial problem was addressed by following a systematic research and development process inside the DSR framework. The real-world problem was analysed, converted to an abstraction in the form of a functional model (with process flow and architecture), investigated by using available literature with topics shown in the validation matrix, creatively solved by using design methodology, and finally validated by means of testing and evaluation.

Validation, in this research context, is thus the combination of validation of each information source, research methodology, deductions made from literature, creative input in the form of design, and final test and verification of artefact characteristics. The electronic artefact was physically tested and thus verified, while the mechanical model was validated from literature (method and knowledge).

### 7.3 Summary

In conclusion, this thesis utilized the DSR research methodology and applied this methodology to a real-world problem, namely the design of an autonomous neutron monitor.

An electronic unit and mechanical model were created after a literature study, and the models and constructs were put through a process of rigor for the purpose of testing and validation. The electronic construct functioned within specification, while the mechanical (theoretical model) was validated from literature.
The contribution of this research was not limited to the creation of a physical artefact, but also the addition to a knowledge base of design processes and methods. The following artefacts were delivered:

Primary artefacts:

- A LPT-NM DAS was constructed (implementation);
- A mechanical model was derived (theoretical).

Meta-artefacts (knowledge base):

- Low-temperature electronic design;
- Low-temperature mechanical design;
- Low-power electronic design;
- Low-power firmware design;
- Application of DSR in this context.

To summarize, the application of DSR to the synthesis and evaluation of an autonomous neutron monitor resulted in a solution that addressed the initial real-world problem. The scope of this research limited the neutron monitor’s implementation to an electronic data acquisition unit that had to function at low temperature and with low power consumption. These requirements were successfully addressed. In addition, a theoretical model was put forward for future development – this was not part of the initial scope but had to be done in order to validate the temperature constraints (i.e. feasibility of operation) placed on the electronic unit. Meta-artefacts, resulting from this study, were defined to ensure continuity of this research in future research and development. Finally, the use of a validation matrix demonstrates how this research was successfully applied to provide a solution to the initial research challenge.
Appendix A – 3D mechanical models

Figure A-1 System enclosed volume model
Figure A-2 Front view LPT-NM electronics 3D model

Figure A-3 Back view LPT-NM electronics 3D model
Appendix B – Electronic models

LPT-NM circuit diagrams

Figure B-1 MCU connections schematic

Figure B-2 MCU voltage filter capacitors schematic
Figure B-3 USB and GPS schematics

Figure B-4 MMC and temperature sensor schematics
Figure B-5 High-voltage module schematics

Figure B-6 High-voltage low-pass filter network
Figure B-7 2.8V DC/DC converter module schematic

Figure B-8 6.1 V DC/DC converter module schematic

Figure B-9 Heating circuit schematic

Figure B-10 Amplifier circuit schematic
Appendix C – Pre-amplifier characteristics

To validate the functioning pre-amplifier design, the pulse height analysis was measured for both a BF\textsuperscript{3} and He\textsuperscript{3} counters, as shown below. These pulse height distributions compare favourably with previous results and serve as validation for the pre-amplifier design.

![Pre-amplifier pulse-height distributions](image)

**Figure C-1** Pre-amplifier pulse-height distributions
Appendix D – Converter efficiencies

DC/DC converter efficiency graphs

![2.8 V Buck-converter efficiency curve](image1.png)

Figure D-1 2.8 V Buck-converter efficiency curve

![6.1 V Buck-converter efficiency curve](image2.png)

Figure D-2 6.1 V Buck-converter efficiency curve
Appendix E – Microprocessor task timing

Figure E-1 Temperature sample MCU process timing

Figure E-2 Pressure sensor sample MCU process timing
Figure E-1 GPS calendar synchronize MCU process timing
8 Bibliography


